Dual 16 Bit, 1.25GSPS Signal Processing DAC with JESD204A Serial Interface

Preliminary Technical Data

AD9128

FEATURES

Low power: 1.4 W @ 1.0 GSPS, 1.2 @ 614 MSPS, full operating conditions
Data Interface through Four 3.125Gbps JESD204A compliant data lanes
Single carrier WCDMA ACLR = 76 dBc @ 80 MHz IF
Analog output: adjustable 8.7 mA to 31.7 mA, RL = 25 Ω to 50 Ω
2x/4x/8x interpolator/complex modulator allows carrier placement anywhere in DAC bandwidth
Multi-chip synchronization interface with latency locking
High performance, low noise PLL clock multiplier
Digital inverse sinc filter
56-lead, exposed paddle LFCSP package

APPLICATIONS

Wireless infrastructure
Transmit diversity
Wideband communications: LMDS/MMDS, point-to-point

GENERAL DESCRIPTION

The AD9128 is a dual, 16-bit, high dynamic range, digital-to-analog converter (DAC) that provides a sample rate of 1.25 GSPS, permitting a multi-carrier generation up to the Nyquist frequency. The AD9128 includes features optimized for direct conversion transmit applications, including complex digital modulation, and gain and offset compensation. The DAC outputs can interface seamlessly with Analog Devices' quadrature modulators such as the ADL537x Broadband QMOD series.

The AD9128 incorporates four high-speed serial data lanes reducing the interface connections between the DAC and its digital companion chip compared with CMOS or LVDS parallel interfaces. The serial interfaces are capable of receiving data with voltage swings of 200 to 700mV$_{p-p}$. With 3 dB of typical receiver equalization, the receiver is capable of capturing data sent across 0 to 20 cm traces on an FR4 board. The AD9128 also features multi-chip deterministic latency capability, allowing multiple dual DACs to be in alignment with one another.

A serial port interface provides read/write access to on-chip registers. Full-scale output current is programmable over a range of 8.5 mA to 31 mA. TheAD9128 operates on 1.8 V and 3.3 V supply rails.

PRODUCT HIGHLIGHTS

1. Small package size 8mm x 8mm footprint
2. Fewer pins for data input word width with only Four JESD204A data lines
3. Ultra low noise and intermodulation distortion (IMD) enables high quality transmission of wideband signals from baseband to high intermediate frequencies.
4. A proprietary DAC output switching technique enhances dynamic performance.

TYPICAL SIGNAL CHAIN

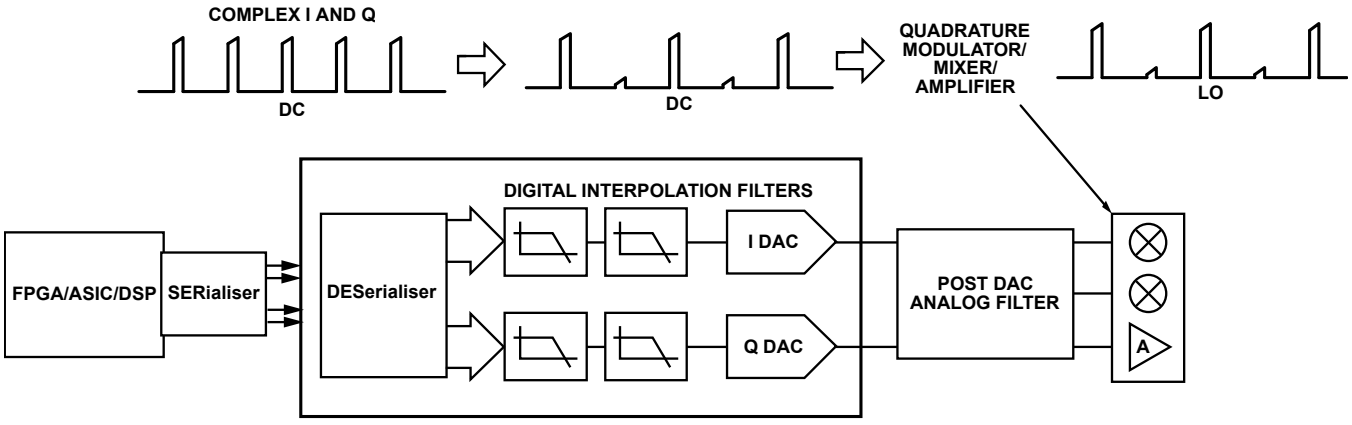

Figure 1. Typical signal chain with simplified block diagram of the AD9128

Rev. PrI

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FUNCTIONAL BLOCK DIAGRAM

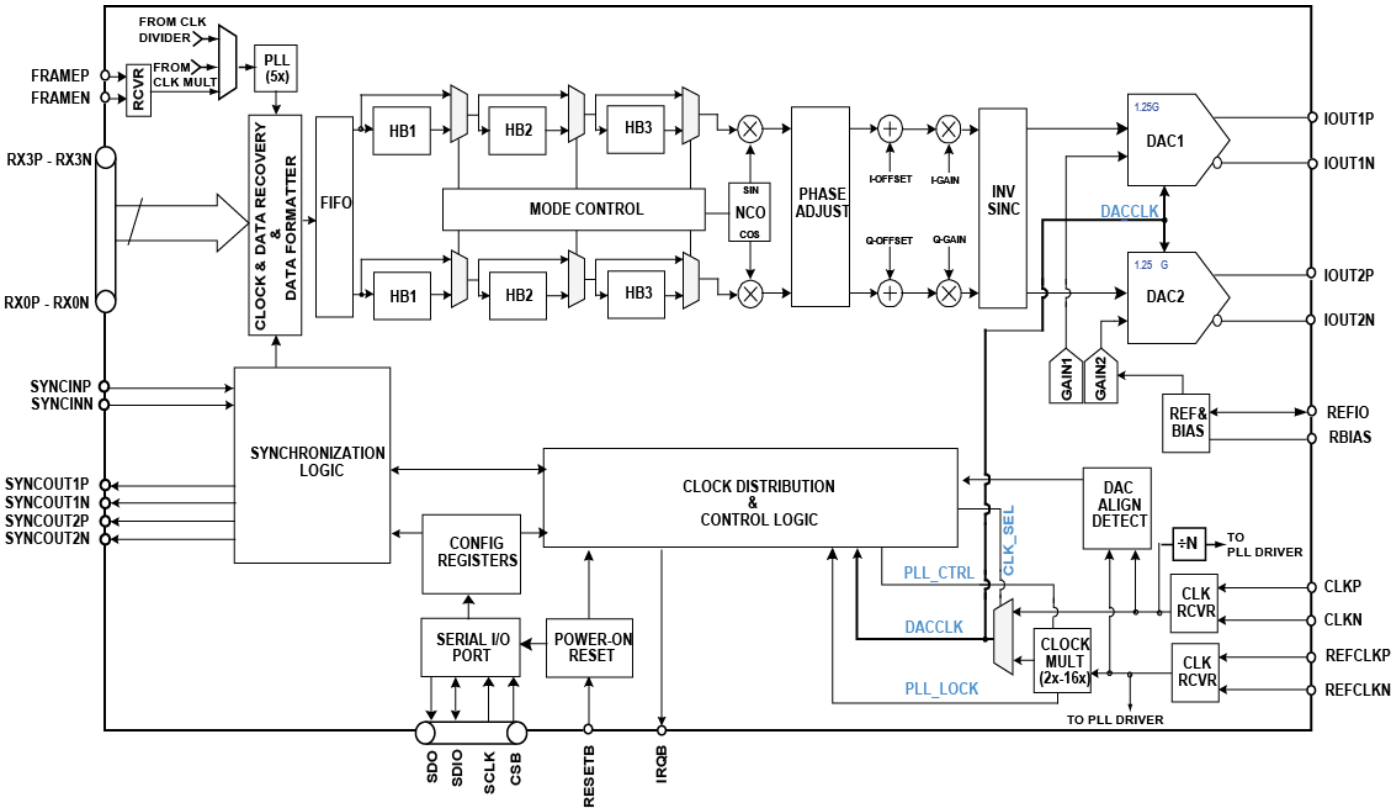


TABLE OF CONTENTS

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, IOVDD = 3.3V, DVDD18 = SVDD = PLLVDD = VTTVDD = CVDD18 =1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 1. DC Specifications

Parameter	Min	Typ	Max	Unit
RESOLUTION		16		Bits
ACCURACY				
Differential Nonlinearity (DNL)		TBD		LSB
Integral Nonlinearity (INL)		TBD		LSB
MAIN DAC OUTPUTS				
Offset Error	TBD	0	TBD	% FSR
Gain Error (with Internal Reference)	TBD	TBD	TBD	% FSR
Full-Scale Output Current[1]	TBD	TBD	TBD	mA
Output Compliance Range	TBD		TBD	V
Output Resistance		10		MΩ
Gain DAC Monotonicity		Guaranteed		
Settling Time to Within ±0.5 LSB		20		ns
MAIN DAC TEMPERATURE DRIFT				
Offset		0.04		ppm/°C
Gain		100		ppm/°C
Reference Voltage		30		ppm/°C
REFERENCE				
Internal Reference Voltage		1.2		V
Output Resistance		5		kΩ
VTT - SERDES Lane Input Termination Voltage	0.8		1.3	V
ANALOG SUPPLY VOLTAGES				
AVDD33	3.13	3.3	3.47	V
CVDD18	1.71	1.8	1.89	V
DIGITAL SUPPLY VOLTAGES				
DVDD18	1.71	1.8	1.89	V
IOVDD	1.71	1.8/3.3	3.47	V
VTTVDD	1.71	1.8	1.89	V
PLLVDD	1.71	1.8	1.89	V
SVDD	1.71	1.8	1.89	V
POWER CONSUMPTION				
2× Mode, f_{DAC} = 614.4 MSPS, 4 lanes @ 3072 MHz, PLL Off, Fs/4		TBD		mW
4× Mode, f_{DAC} = 1228.8 MSPS, 4 lanes @ 3072 MHz, NCO On		TBD		mW
4× Mode, f_{DAC} = 983 MSPS, 4 lanes @ 2457.6 MHz, NCO On		TBD		mW
AVDD33		TBD		mA
CVDD18		TBD		mA
DVDD18		TBD		mA
VTTVDD		TBD		mA
SVDD		TBD		mA
PLLVDD		TBD		mA
Power-Down Mode		TBD		mW
Power Supply Rejection Ratio, AVDD33	−0.3		+0.3	% FSR/V
OPERATING RANGE	−40	+25	+85	°C

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, IOVDD = 3.3V, DVDD18 = SVDD = PLLVDD = VTTVDD = CVDD18 =1.8 V, I_{OUTFS} = 20 mA, maximum sample rate, unless otherwise noted.

Table 2. Digital specifications

Parameter	Conditions	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL					
Input V_{IN} Logic High	IOVDD = 1.8 V	1.2			V
Input V_{IN} Logic High	IOVDD = 2.5 V	1.6			V
Input V_{IN} Logic High	IOVDD = 3.3 V	2.0			V
Input V_{IN} Logic Low	IOVDD = 1.8 V			0.6	V
Input V_{IN} Logic Low	IOVDD = 2.5 V, 3.3 V			0.8	V
CMOS OUTPUT LOGIC LEVEL					
Output V_{OUT} Logic High	IOVDD = 1.8 V	1.4			V
Output V_{OUT} Logic High	IOVDD = 2.5 V	1.8			V
Output V_{OUT} Logic High	IOVDD = 3.3 V	2.4			V
Output V_{OUT} Logic Low	IOVDD = 1.8 V, 2.5 V, 3.3 V			0.4	V
JESD204 DATA INTERFACE					
Number of JESD204A lanes				4	Lanes
JESD204A Serial interface speed	Per lane	1.5		3.125	Gbps
DAC sample rate	4x interpolation			1.25	GSPS
Input Data rate	All 4 lanes enabled			312.5	MSPS
RX0P/RX0N, RX1P/RX1N, RX2P/RX2N, RX3P/RX3N	Current Mode Logic (CML) Compliant, per JESD204				
Input Impedance	Terminated to a Common Voltage (VTT) with an Integrated Resistor		50		Ω
DAC CLOCK INPUT (DACCLKP, DACCLKN)					
Differential Peak-to-Peak Voltage		100	500	2000	mV
Common-Mode Voltage	Self biased input, ac coupled		1.25		V
Receiver Differential Input Impedance, R_{IN}		TBD		TBD	Ω
Maximum Clock Rate			1250		MHz
REFCLK INPUT (REFCLKP, REFCLKN)					
Differential Peak-to-Peak Voltage		100	500	2000	mV
Common-Mode Voltage			1.25		V
REFCLK Frequency (PLL Mode)	1 GHz ≤ f_{VCO} ≤ 2.1 GHz	15.625		312	MHz
FRAME INPUT (FRAMEP, FRAMEN)					
Differential Peak-to-Peak Voltage		100	500	2000	mV
Common-Mode Voltage			1.25		V
SYNCIN INPUT (SYNCINP, SYNCINN)					
Input Voltage Range, V_{IA} or V_{IB}		825		1575	mV
Input Differential Threshold, V_{IDTH}		−100		+100	mV
Input Differential Hysteresis, $V_{IDTHH} – V_{IDTHL}$			20		mV
Receiver Differential Input Impedance, R_{IN}		80		120	Ω
SYNCOUT OUTPUTS (SYNCOUT1P, SYNCOUT1N and SYNCOUT2P, SYNCOUT2N)					
Output Voltage High, V_{OA} or V_{OB}				1375	mV
Output Voltage Low, V_{OA} or V_{OB}		1025			mV
Output Differential Voltage, $\|V_{OD}\|$		150	200	250	mV
Output Offset Voltage, V_{OS}		1150		1250	mV
Output Impedance, Single-Ended, R_O		80	100	120	Ω

SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (SCLK)			20	MHz
Minimum Pulse Width High (t_{PWH})			25	ns
Minimum Pulse Width Low (t_{PWOL})			25	ns
Setup Time, SDI to SCLK (t_{DS})		1.9		ns
Hold Time, SDI to SCLK (t_{DH})		0.2		ns
Data Valid, SDO to SCLK (t_{DV})		2.3		ns
Setup Time, $\overline{CS}$ to SCLK (t_{DCSB})		1.4		ns

DIGITAL INPUT DATA TIMING

Table 3. Input data timing specifications

Parameter	Min	Typ	Max	Unit
LATENCY (DACCLK Cycles)				
1× Interpolation (With or Without Modulation)		TBD		Cycles
2× Interpolation (With or Without Modulation)		TBD		Cycles
4× Interpolation (With or Without Modulation)		TBD		Cycles
8× Interpolation (With or Without Modulation)		TBD		Cycles
Inverse Sinc		TBD		Cycles
Fine Modulation		TBD		Cycles
Power-Up Time		TBD		ms

AC SPECIFICATIONS

TMIN to TMAX, AVDD33 = 3.3 V, IOVDD = 3.3V, DVDD18 = SVDD = PLLVDD = VTTVDD = CVDD18 =1.8 V, IOUTFs = 20 mA, maximum sample rate, unless otherwise noted.

Table 4. AC Specifications

Parameter	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)				
f_{DAC} = 100 MSPS, f_{OUT} = 20 MHz		TBD		dBc
f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		TBD		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 70 MHz		TBD		dBc
f_{DAC} = 800 MSPS, f_{OUT} = 70 MHz		TBD		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)				
f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz		TBD		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 60 MHz		TBD		dBc
f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		TBD		dBc
f_{DAC} = 800 MSPS, f_{OUT} = 100 MHz		TBD		dBc
NOISE SPECTRAL DENSITY (NSD) EIGHT-TONE, 500 kHz TONE SPACING				
f_{DAC} = 200 MSPS, f_{OUT} = 80 MHz		TBD		dBm/Hz
f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz		TBD		dBm/Hz
f_{DAC} = 800 MSPS, f_{OUT} = 80 MHz		TBD		dBm/Hz
W-CDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER				
f_{DAC} = 491.52 MSPS, f_{OUT} = 10 MHz		TBD		dBc
f_{DAC} = 491.52 MSPS, f_{OUT} = 122.88 MHz		TBD		dBc
f_{DAC} = 983.04 MSPS, f_{OUT} = 122.88 MHz		TBD		dBc
W-CDMA SECOND ACLR, SINGLE CARRIER				
f_{DAC} = 491.52 MSPS, f_{OUT} = 10 MHz		TBD		dBc
f_{DAC} = 491.52 MSPS, f_{OUT} = 122.88 MHz		TBD		dBc
f_{DAC} = 983.04 MSPS, f_{OUT} = 122.88 MHz		TBD		dBc

ABSOLUTE MAXIMUM RATINGS

Table 5. Absolute Maximum Ratings

Parameter	With Respect To	Rating
AVDD33	AVSS, EPAD, CVSS, DVSS	−0.3 V to +3.6 V
IOVDD	AVSS, EPAD, CVSS, DVSS	−0.3 V to +3.6 V
DVDD18, CVDD18, SVDD, PLLVDD, VTTVDD	AVSS, EPAD, CVSS, DVSS	−0.3 V to +2.1 V
AVSS	EPAD, CVSS, DVSS	−0.3 V to +0.3 V
EPAD	AVSS, CVSS, DVSS	−0.3 V to +0.3 V
CVSS	AVSS, EPAD, DVSS	−0.3 V to +0.3 V
DVSS	AVSS, EPAD, CVSS	−0.3 V to +0.3 V
BIAS_RES, REFIO, IOUT1P/IOUT1N, IOUT2P/IOUT2N	AVSS	−0.3 V to AVDD33 + 0.3 V
RXN[3:0]/RXP[15:0], JESD_FRAMEP/JESD_FRAMEN	EPAD, DVSS	−0.3 V to DVDD18 + 0.3 V
DACCLKP/DACCLKN, REFCLKP/REFCLKN	CVSS	−0.3 V to CVDD18 + 0.3 V
$\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, $\overline{\text{CS}}$, SCLK, SDIO, SDO	EPAD, DVSS	−0.3 V to IOVDD + 0.3 V
Junction Temperature		125°C
Storage Temperature Range		−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
56 pin LFCSP	TBD	TBD	TBD	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

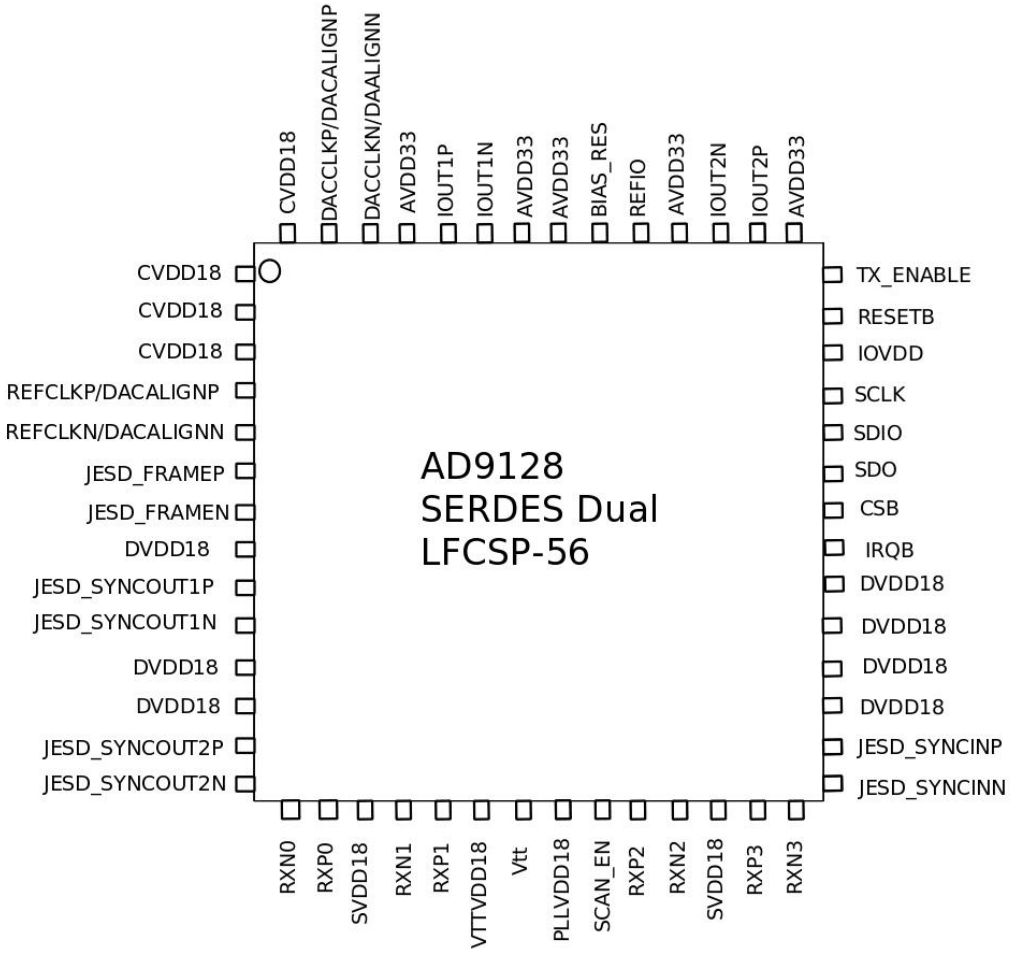


Figure 2.

Table 7. Pin List and Description

Pin	Name	Description	I/O Pin
1	CVDD18	1.8V Clock Supply – Analog Clock Supply	I
2	CVDD18	1.8V Clock Supply – Analog Clock Supply	I
3	CVDD18	1.8V Clock Supply – PLL Supply (DAC clock generator)	I
4	REFCLKP/DACALIGNP	If PLL enabled, Reference Clock positive, else DAC align positive[1]. REFCLKP can be AC coupled. DACALIGNP cannot be AC coupled and needs 100 ohm (LVDS) resistor	I
5	REFCLKN/DACALIGNN	If PLL enabled, Reference Clock negative, else DAC align negative[1]. REFLCKN can be AC coupled. DACALIGNN cannot be AC coupled and needs 100 ohm (LVDS) resistor	I
6	JESD_FRAMEP	JESD204A Compliant frame clock, positive. Can be AC coupled.	I
7	JESD_FRAMEN	JESD204A Compliant frame clock, negative. Can be AC coupled.	I
8	DVDD18	1.8V Digital Supply – for frame clock and timing DLL.	I
9	JESD_SYNCOUT1P	JESD204A SYNC Signal, Positive. LVDS compliant.	O
10	JESD_SYNCOUT1N	JESD204A SYNC Signal, Negative. LVDS compliant.	O
11	DVDD18	1.8V Digital Supply (Core)	I

[1] Single Edge DAC Alignment input if PLL is disabled. LVDS resistor required between this pin and REFCLK in align mode.

12	DVDD18	1.8V Digital Supply (Core)	I
13	JESD_SYNCOUT2P	JESD204A SYNC Signal Auxiliary, Positive. LVDS compliant.	O
14	JESD_SYNCOUT2N	JESD204A SYNC Signal Auxiliary, Negative. LVDS compliant.	O
15	RXN0	Serial Channel input 0, Negative. CML compliant. 50 ohm-terminated to Vtt pin voltage. Can be AC coupled. Resistance calibrated.	I
16	RXP0	Serial channel input 0, Positive. CML compliant. 50 ohm-terminated to Vtt pin voltage. Can be AC coupled. Resistance calibrated.	I
17	SVDD18	1.8V Deserializer Supply for RX0 and RX1	I
18	RXN1	Serial channel input 1, Negative. CML compliant. 50 ohm-terminated to Vtt pin voltage. Can be AC coupled. Resistance calibrated.	I
19	RXP1	Serial channel input 1, Positive. CML compliant. 50 ohm-terminated to Vtt pin voltage. Can be AC coupled. Resistance calibrated.	I
20	VTTVDD18 (SVDD18)	1.8V Deserializer supply (Vtt and bias generation supply)	I
21	VTT	SERDES Lane Input Termination Voltage. Used for supplying external termination voltage. Load should be < 100pF if internal voltage is used.	I
22	PLLVDD18	1.8V PLL Supply	I
23	DVSS (GND)	Tied to ground	I
24	RXP2	Serial channel input 2, Positive . CML compliant. 50 ohm-terminated to Vtt pin voltage. Can be AC coupled. Resistance calibrated.	I
25	RXN2	Serial channel input 2, Negative. CML compliant. 50 ohm-terminated to Vtt pin voltage. Can be AC coupled. Resistance calibrated.	I
26	SVDD18	1.8V Deserializer Supply for Rx2 and RX3	I
27	RXP3	Serial channel input 3, Positive. CML compliant. 50 ohm-terminated to Vtt pin voltage. Can be AC coupled. Resistance calibrated.	I
28	RXN3	Serial channel input 3, Negative . CML compliant. 50 ohm-terminated to Vtt pin voltage. Can be AC coupled. Resistance calibrated.	I
29	JESD_SYNCINN	JESD204A SYNC signal input, Negative. LVDS compliant SYNC input with internal differential termination only. Resistance calibrated.	I
30	JESD_SYNCINP	JESD204A SYNC signal input, Positive. LVDS compliant SYNC input with internal differential termination only. Resistance calibrated.	I
31	DVDD18	1.8V Digital Supply (Core)	I
32	DVDD18	1.8V Digital Supply (Core)	I
33	DVDD18	1.8V Digital Supply	I
34	DVDD18	1.8V Digital Supply	I
35	IRQB	Interrupt Request. Open Drain, Active Low Output	O
36	CSB	Serial Port Chip Select. Active Low (CMOS levels w.r.t. IOVDD)	I
37	SDO	Serial Port Data Output (CMOS levels w.r.t. IOVDD)	O
38	SDIO	Serial Port Data Input/Output (CMOS levels w.r.t. IOVDD)	I/O
39	SCLK	Serial Port Clock Input (CMOS levels w.r.t. IOVDD)	I
40	IOVDD	1.8V – 3.3V Serial Port Supply	I
41	RESETB	Reset. Active Low. (CMOS levels w.r.t. IOVDD)	I
42	TXENABLE	Transmit Enable Function pin, programmable parameters through SPI.	I
43	AVDD33	3.3V Analog Supply – DAC supply	I
44	IOUT2P	Q DAC Positive Current Output	O
45	IOUT2N	Q DAC Negative Current Output	O
46	AVDD33	3.3V Analog Supply	O
47	REFIO	Voltage Reference. Nominally 1.2V output. Should be decoupled to Analog Ground.	I
48	BIAS_RES	External reference resistance. Used to set LVDS swing, DAC full-scale current, and deserializer input termination. Place 10K ohm resistor to analog ground.	I

49	AVDD33	3.3V Analog Supply	I
50	AVDD33	3.3V Analog Supply	I
51	IOUT1N	I DAC Negative Current Output	O
52	IOUT1P	I DAC Positive Current Output	O
53	AVDD33	3.3V Analog Supply	I
54	DACCLKN/DACALIGNN	DAC Clock Negative input if PLL disabled. DAC Alignment Negative input if PLL is enabled. DACCLKN can be AC coupled. DACALIGNN cannot be AC coupled and needs 100 ohm (LVDS) resistor	I
55	DACCLKP/DACALIGNP	DAC Clock Positive input if PLL disabled. DAC Alignment Positive input if PLL is enabled. DACCLKP can be AC coupled. DACALIGNP cannot be AC coupled and needs 100 ohm (LVDS) resistor	I
56	CVDD18	1.8V Supply – Clock Supply Voltage	I

TYPICAL PERFORMANCE CHARACTERISTICS

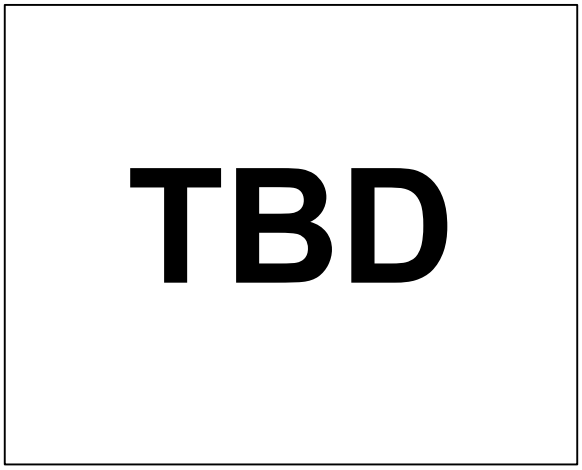


Figure 3

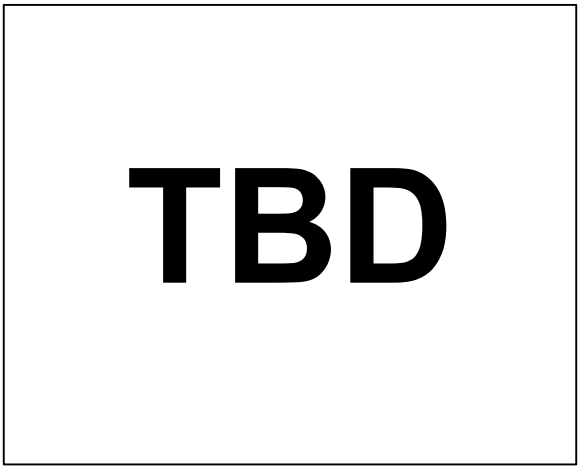


Figure 6

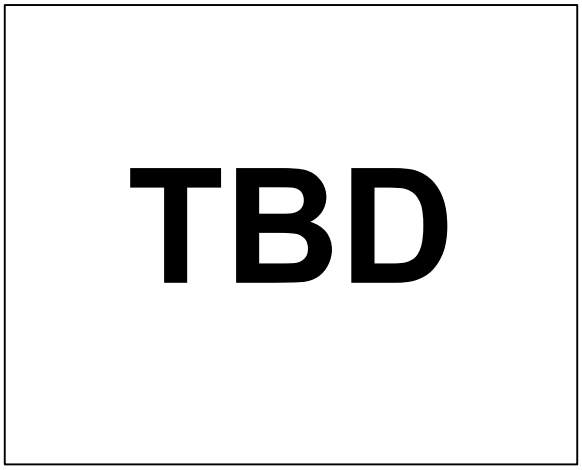


Figure 4

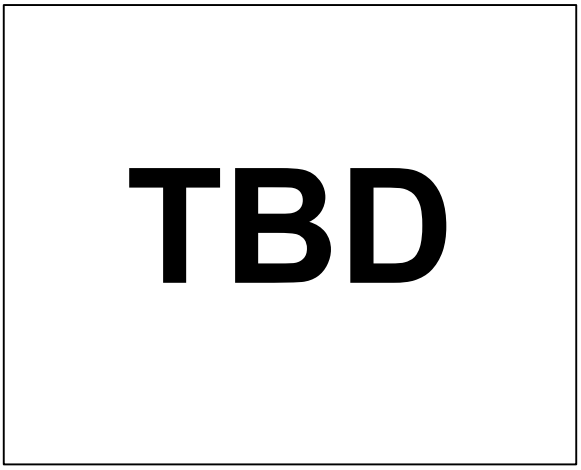


Figure 7

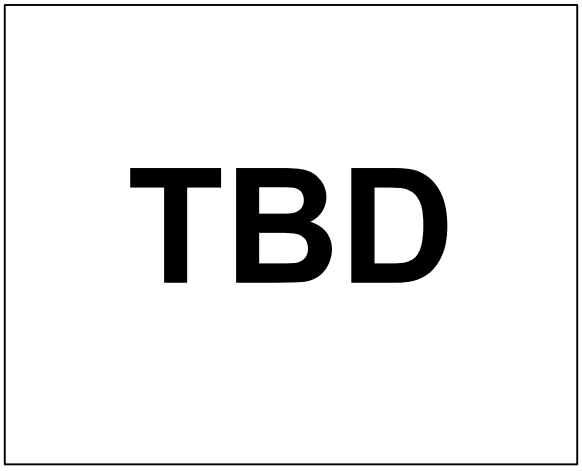


Figure 5

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Offset Error
Offset error is the deviation of the output current from the ideal of 0 mA. For IOUT1P, 0 mA output is expected when all inputs are set to 0. For IOUT1N, 0 mA output is expected when all inputs are set to 1.

Gain Error
Gain error is the difference between the actual and ideal output span. The actual span is determined by the difference between the output when all inputs are set to 1 and the output when all inputs are set to 0.

Output Compliance Range
The output compliance range is the range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree Celsius. For reference drift, the drift is reported in ppm per degree Celsius.

Power Supply Rejection (PSR)
PSR is the maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Spurious Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal within the dc to Nyquist frequency of the DAC. Typically, energy in this band is rejected by the interpolation filters. This specification, therefore, defines how well the interpolation filters work and the effect of other parasitic coupling paths on the DAC output.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Interpolation Filter
If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around f_{DAC} (output data rate) can be greatly suppressed.

Adjacent Channel Leakage Ratio (ACLR)
ACLR is the ratio in decibels relative to the carrier (dBc) between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection
In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

Current Mode Logic (CML)

CML is a differential digital logic family. Signal transmission is point-to-point, unidirectional and terminated at the destination with 50 Ω resistors to a voltage, VTT, on both differential lines. CML is the physical layer for JESD204.

THEORY OF OPERATION

The AD9128 is a 16-bit Dual DAC with a SERDES interface that is fully compliant with the JESD204A specifications. Figure *8* shows a top-level diagram of the AD9128. Four high-speed serial lanes carry data with a maximum speed of 3.125Gbps, resulting in a 312.5 MSPS (maximum) input data rate for each of the two DACs. The AD9128 can be configured to operate in 1, 2 or 4 JESD204A lane modes, depending on the required DAC input data rate. It can also operate in single DAC mode, with either 1-lane or 2-lane mode.

The two DACs can operate as I and Q channels in a direct conversion transmitter. Or as two independent DACs running at the same DAC sampling rate. The digital data-path of the AD9128 offers four interpolation modes (1X, 2X, 4X or 8X) through three half-band filters with a maximum DAC sampling rate of 1.25 GSPS.

F_{DAC} is the DAC sampling frequency. The input signal data-rate for both DACs is F_{DAC} ÷ the interpolation factor.

For I/Q applications a Numerically Controlled Oscillator (NCO) provides a means for modulating the signal with a programmable carrier signal. The NCO generates the carrier signal for a complex modulator in the digital data path. The resolution of the NCO is 32 bits, allowing the signal to be placed in the output spectrum with very fine resolution. The **AD9128 Startup** Sequence). The following sections describe elements of the AD9128 in detail.

AD9128 also features coarse modulation. Coarse modulation up converts a digital signal centered at DC center frequency of $F_{DAC}/4$. This option consumes significantly less power compared with the NCO modulation approach. Digital gain, offset and phase compensation are included in the AD9128 to help with unwanted sideband suppression in direct conversion transmitters. An inverse Sinc filter is provided to compensate for DAC output sinc-related roll-off.

The DAC Clock (DACCLK) can be sourced externally. Or generated on chip using a PLL synthesizer with externally supplied reference signal.

The AD9128 DAC core provides a fully differential current output with a nominal full-scale current of 20mA. The full-scale current is user adjustable between 8.7mA and 31.7mA. The differential current outputs are complementary.

The AD9128 is capable of multi-chip synchronization and can both synchronize devices and establish deterministic latency (latency locking) among multiple AD9128 devices. The latency for each of the DACs remains constant from link establishment to link establishment.

A SPI interface provides read and write access to registers. The various functional blocks and the data interface need to be setup in a specific sequence for proper operation (See section

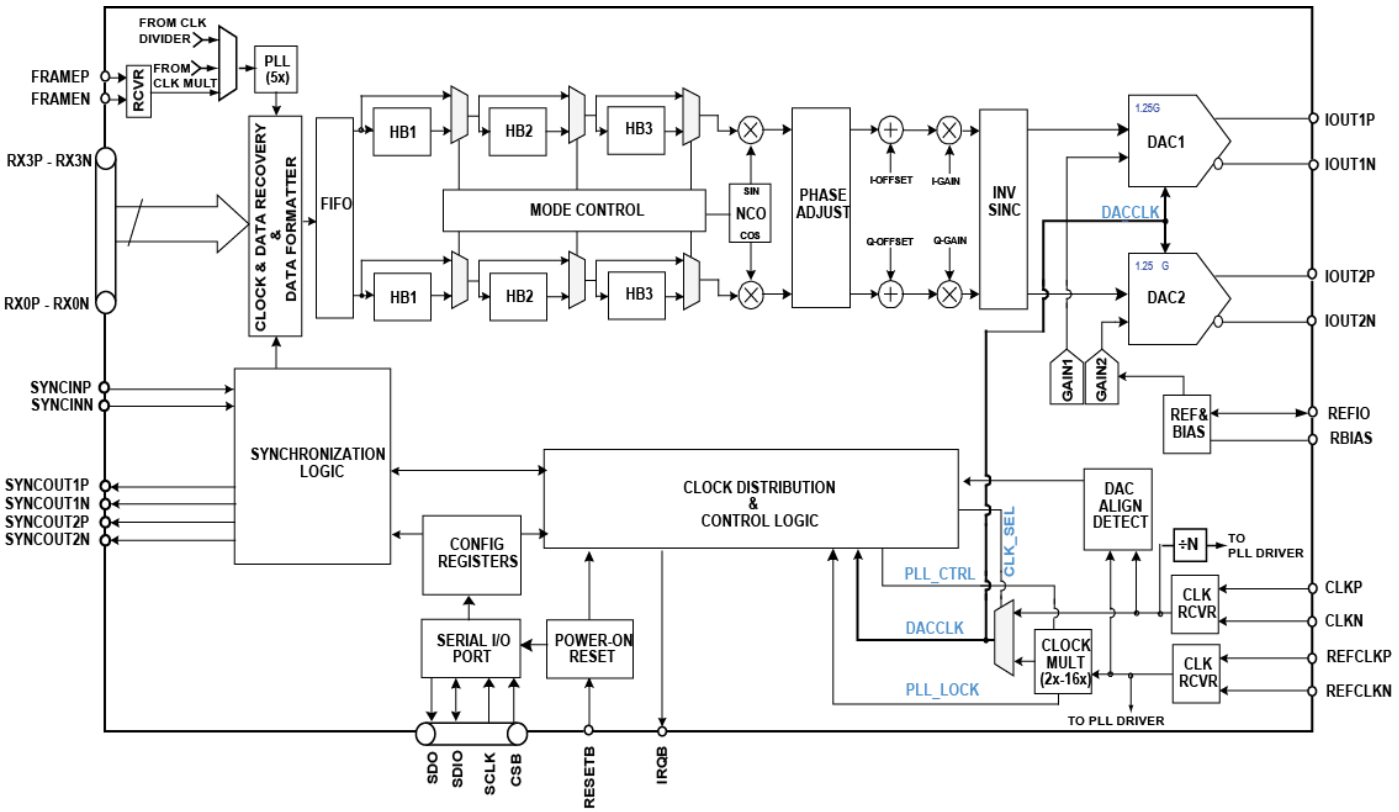


Figure 8. AD9128 Functional Block Diagram

HIGH SPEED SERIAL DATA INTERFACE

The AD9128 has four JESD204A data ports that receive data for both I and Q transmit paths. Figure *9* describes the communication layers implemented in the AD9128 for each high speed serial data interface to recover the clock, descramble and deserialize the data before it is sent to the Digital Signal Processing section of the AD9128. If a lower data speed is acceptable the part can be configured to operate with either two or one JESD204A lanes. The maximum data speed is directly linked to the number of lanes used. In the 4 lane, 2 lane and 1 lane configurations, the maximum supported data speeds are 312.5 MSPS, 156.25 MSPS and 78.125 MSPS respectively.

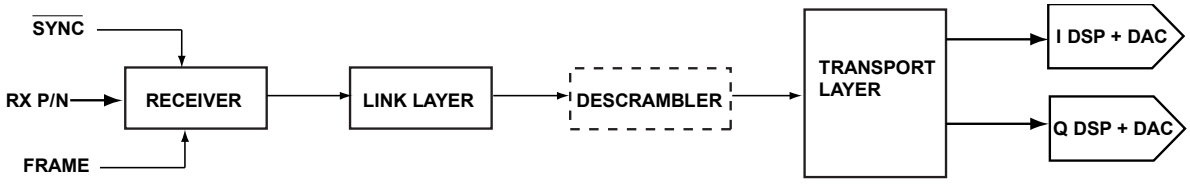


Figure 9. Functional block diagram of Serial receiver

As the AD9128 can operate with more than one active high speed serial data lane, both achieving synchronization and handling loss of synchronization of the lanes are very important. To simplify the interface to the companion digital chip, theAD9128 designates one master signal (SYNCb) as far as multiple lane synchronization is concerned. If one lane loses synchronization, a resynchronization request is sent to the transmitter and the transmitter stops sending data to all lanes until resynchronization has been achieved.

RECEIVER CIRCUIT

The AD9128 provides four 1.8V differential serial input interfaces compliant with the JESD204A specifications. These interfaces can accept signals at frequencies up to 3.125Gbps using the input topology in Figure *10*.

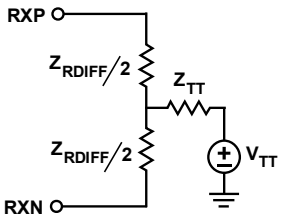


Figure 10. Receiver line termination

The receiver eye mask in Figure 11 specifies the signal amplitude and jitter tolerance for the AD9128 High Speed Serial Data Interface receiver.

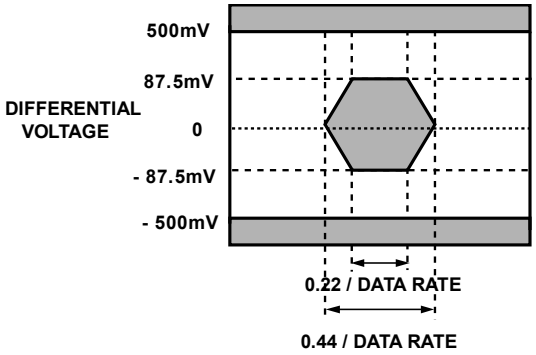


Figure 11. Receiver Eye Mask

The receiver is equipped with a Clock/Data Recovery circuit (CDR) based on a PLL. The PLL effectively multiplies the Frame clock input by 5 X F (F=Number of bytes per frame) and the CDR synchronizes the phase used to sample the data on each serial lane independently. This independent phase adjustment per serial interface ensures accurate data sampling and eases the implementation of multiple serial interfaces on a PCB. A byte rate PLL clock is then used in the link layer, descrambler and transport layers to deserialize the serial input and provide data to the DAC inputs.

LINK LAYER

The AD9128 can operate with more than one active high speed serial data interface. Link layer communications such as code group synchronization, frame alignment and frame synchronization are handled by all four lanes. However, the configuration data is always checked only on a single logical high speed serial data interface: LN0. This logical serial interface can be connected to any of the four JESD204A physical receivers RXn. It is important to note that logical LN0 must be active in all modes of operation.

The AD9128 decodes 8B/10B control characters allowing marking of start and end of frame and alignment between serial lanes. The AD9128 serial interface can issue a synchronization

request by setting the SYNCb pin low. The synchronization protocol follows the JESD204A standard. When a stream of 8 consecutive /K/ symbols is received, the AD9128 deactivates the synchronization request by setting SYNCb pin high and waits for the transmitter to issue an Initial Lane Alignment Sequence (ILAS).

DESCRAMBLER

The AD9128 provides an optional descrambler block using a self-synchronous descrambler with polynomial: $1 + x^{14} + x^{15}$.

Data scrambling can be selected at the transmitter to reduce spectral peaks that would be produced when the same data octets repeat from frame to frame. Another advantage of scrambling is that it makes the spectrum data independent so that possible frequency-selective effects on the electrical interface will not cause data-dependent errors.

TRANSPORT LAYER

The transport layer maps the incoming descrambled data to DAC samples. It provides control of the JESD204A parameters shown in Table 8.

Table 8. JESD204A Transport Layer Parameters

Parameter	Description
F	Number of bytes per frame: 1, 2 or 4 depending on L
K	Number of frame per multi-frame: K = 32 if F=1, K=16 otherwise.
L	Number of lanes per converter device: 1, 2 or 4
M	Number of converter per device = 1, 2

Since the AD9128 uses the Frame input as the reference clock for the deserializer PLL, the Frame input needs to be greater than 50 MHz. A number of transport layer configurations are defined to fit the AD9128 definition, as shown in

Table **9**.

Table 9. JESD204A Configuration Parameters

Parameter	Description
CF	Number of control words per frame clock per link = 0. No control word is embedded with samples
CS	Number of control bits per conversion sample = 0
HD	High density user data format. Used when samples need to be split across lanes. Set to 1 when F=1, 0 otherwise.
N	Converter resolution = 16
N'	Total number of bits per sample = 16

Since the AD9128 has four high speed serial data interfaces, several combinations of lanes per converter can be used depending on the data rate desired.

The AD9128 can also operate in real single-DAC mode. In this case, it can be configured in either 2-lane or 1-lane mode (Note: all 4 lanes cannot be used in single-DAC mode). The maximum input data rate in single-DAC mode is the same as the dual DAC mode (312.5MHz).

Table 10. AD9128 interface speeds

Parameter	Value		
Serial interface speed	3.125Gbps		
Effective serial interface speed	2.5Gbps		
# of lanes used	4	2	1
DAC Data update rate (MHz)	312.5	156.25	78.125

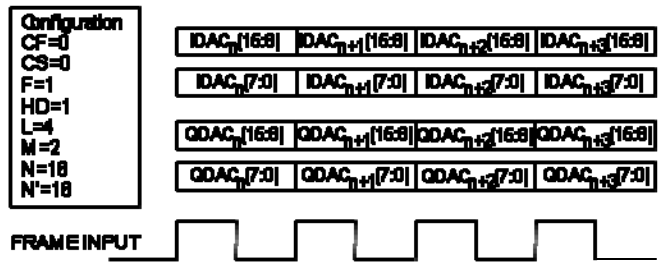


Figure 12. Serial data interface with 4 lanes active

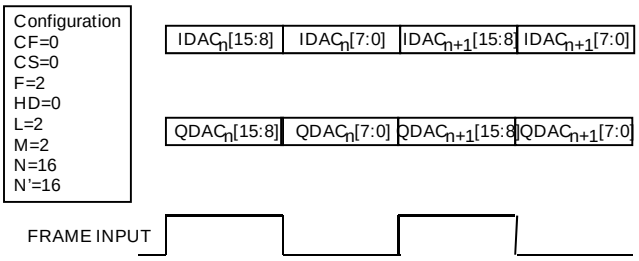


Figure 13. Serial data interface with 2 lanes active

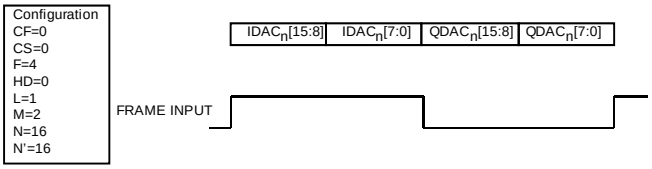


Figure 14. Serial data interface with 1 lane active

JESD204A SERIAL LINK ESTABLISHMENT

A brief summary of the high speed serial link establishment process is given below. Please see the JESD204A Specifications document (reference) for complete details.

1. Code group synchronization
   a. Each receiver must locate K (K28.5) characters in its input data stream

b. Once 8 consecutive K characters have been detected on all link lanes, the receiver block de-asserts the SYNCb signal to the transmitter block.
c. The transmitter captures the change in SYNCb and after a fixed number of frame clocks, starts the Initial Lane Alignment Sequence (ILAS).

2. Initial Lane Alignment Sequence
   a. The main purposes of this phase are to align all the lanes of the link and verify the parameters of the link.
   b. Before the link is established, each of the link parameters is written to the receiver device to designate how data will be sent to the receiver block.
   c. ILAS consists of 4 or more multi-frames. The last character or each multi-frame is a multi-frame alignment character /A/
   d. The first, third, and fourth multi-frames are populated with pre-determined data values. The de-framer uses the final /A/ of each lane to align the ends of the multi-frames within the receiver.
   e. The second multi-frame contains an R (K.28.0), Q(K.28.4), and then data corresponding to the link parameters.
   f. Additional multi-frames can be added to ILAS if needed by the receiver. The AD9128 uses 8 multi-frames in its ILAS. (When alignment scheme or deterministic latency are used.)
   g. After the last /A/ character of the last ILAS multi-frame data begins to be streamed.

3. Data Streaming
   a. In this phase data is streamed from the transmitter block to the receiver block.
   b. Data can be optionally scrambled. Scrambling does not start until the very first octet following the ILAS.
   c. The receiver block processes and monitors the data it receives for errors including:
      i. Bad running disparity (8b/10b error)
      ii. Not in Table (8b/10b error)
      iii. Unexpected control-character
      iv. Bad ILAS
      v. Inter-lane skew error (through character replacement)
   d. If any of these errors exists, it is reported back to the transmitter in one of a few ways
      i. SYNCb assertion: Resynchronization (SYNCb pulled low) is called for at each error. For the first three errors, SYNCb is asserted after an error counter reaches a given error threshold.
      ii. SYNCb reporting: SYNCb is pulsed low for a frame clock period if an error occurs
      iii. Reporting may also be done via interrupt (not covered by the JESD204A specification). See (i) for error thresholds.

FIFO OPERATION

The AD9128 contains several stages of FIFO to deal with the high speed serial data interface protocol and to synchronize the data input with the DAC clock input (See Figure 15).

The FIFO in the SERDES deframer interface is used to synchronize the samples sent on the high speed serial data interface with the deframer clock. This FIFO absorbs timing variations between the data source and the deframer. When the FIFO reaches either full or empty state, it is recommended that the user reset it through Register 35 bit 0 and, if necessary, re-establish the SERDES data link. Note that resetting the SERDES link does not reset the FIFO to half-full automatically.

A second 2 channel x 16-bit wide, 8- word deep FIFO exists in the DAC (datapath FIFO) to absorb timing variations between the DAC clock and the Deframer clock. Figure 16 shows the block diagram of the data path through the FIFO. The data is latched into the device, formatted and then written into the FIFO register determined by the FIFO write-pointer. The value of the write-pointer is incremented every time a new word is loaded into the FIFO. Meanwhile, data is read from the FIFO register determined by the read-pointer and fed into the digital datapath. The value of the read-pointer is updated every rising edge of the internal DAC based data clock. The one exception to this occurs when a resynchronization request is in progress: the write side of the FIFO does not increment and the read side is held in reset at a fixed value. Once the ILAS is completed in the AD9128, then the Datapath FIFO is automatically reset to "half full". During a synchronization request, the DAC outputs are forced to mid-scale and the datapath is flushed. This is done to prevent corrupted data from passing from the DAC.

Valid data will be transmitted through the FIFOs as long as the FIFOs do not overflow or become empty. Nominally, data will be written to the FIFO at the same rate as data is read from the FIFO. This keeps the data level in the FIFO constant. If data is written to the FIFO faster than data is read, the data level in the FIFO increases. If the data is written to the device slower than data is read, the data level in the FIFO decreases.

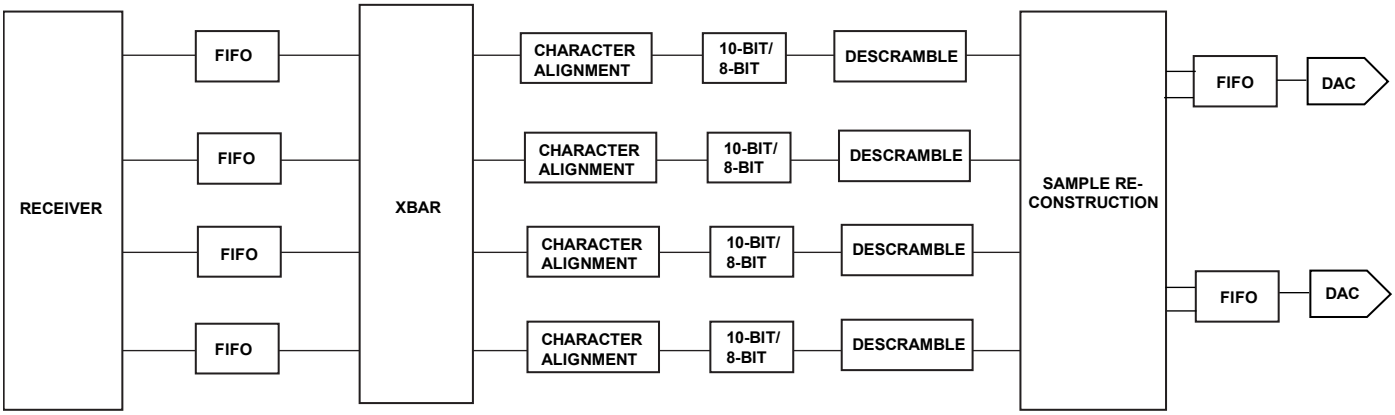


Figure 15. Block Diagram of AD9128 FIFOs

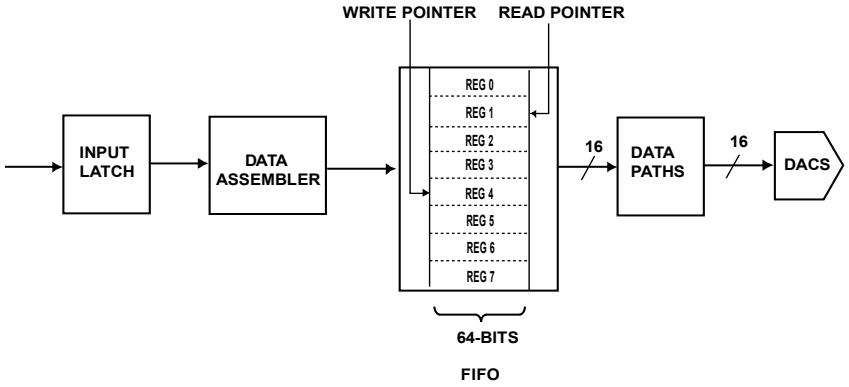


Figure 16 – Block Diagram of Datapath FIFO

FRAME CLOCKING

The frame clock is the master reference for the high speed serial interface of the AD9128. It drives a PLL in the JESD204A part of the system and needs to be set to the input data rate of the system. The user has three options for the frame clock in AD9128:

- Externally sourced through pins JESD_FRAMEP/N: the input should be AC coupled and will be self-biased internally.
- Externally sourced through REFCLKP/N: this is possible only if the internal DAC PLL is used and the supplied reference clock supplied to the PLL (via REFCLKP/N) is at the data rate of the system. (abd equal to the FRAME rate) The input should be AC coupled and will be self-biased internally.
- Internally sourced by using a divided down version of the DAC clock: this helps minimize the number of low frequency clocks in the user system.

The frame clock source is controlled and monitored through register 0x001D.

SERDES PLL

The SERDES PLL generates clocks at half the rate of the serial data rate and supplies them to the Clock and Data Recovery (CDR) block. The SERDES PLL settings are controlled and monitored in the register 0x01E. The PLL divide ratio (register 0x01E, bits [3:0]) is dependent on the F value (number of bytes per frame) of the JESD204A link. The F value of the link (1,2 or 4) should be written to this register. The SERDES PLL can be monitored for lock by reading register 0x01E, bit 6.

The SERDES PLL lock can also be accessed through the interrupt controller by writing Register 0x006, bits 7 and/or 6 high. Bit7 enables the interrupt if the SERDES PLL has lost lock, and Bit6 enables the interrupt if the SERDES PLL is locked. These interrupts can be found by reading register 0x009 bits 7 and 6 (when the interrupt output of the AD9128 falls,).

Note that the SERDES PLL must lock before parameters can be written to the deframer.

CONFIGURING THE JESD204A SERIAL INTERFACE

After the SERDES PLL has been successfully locked, the Deserializer SPI is available and can be verified by reading register 0x02 bit 0. The Deserializer SPI is a synchronous read/write SPI (See section *Serial Peripheral Interface* for SPI interface details). It is addressed through the long addressing mode (default for the AD9128). The addresses for this part of the circuit range from 0x100-0x17F.

Input termination

The AD9128 will auto-calibrate to 50 ohms termination on power-up as register 0x010 bit 5 has a default setting of high. The auto-calibrated value found will be held constant until bit 5 is disabled. Alternatively, a manual calibration value can be entered through register 0x011 bit 3:0 (highest resistor value is 0000 and lowest value is 1111). Manual calibration requires register 0x10 bit5 to be low and 0x11 bit4 to be high. All settings for input termination can be setup and controlled through registers 0x010 and 0x011.

The input termination voltage of the DAC can be sourced either externally or internally:

- External: An external voltage can be driven through the VTT pin. In order to support DC compliance, its value should match the common mode voltage of the CML driver at the transmitter. It may be bypassed at the pin to local ground.
- Internal: The termination voltage can be supplied internally by enabling register 0x010 bit 4. The VTT buffer drives both the internal VTT termination and the VTT pin. The termination voltage value can be set through register 0x010 its 3:0. In this case, the VTT pin should not be bypassed to ground. As in option 1, to meet DC compliance, the value of the voltage should be chosen to be close to the value of the CML driver output common-mode. This will ensure minimum power consumption.

For AC coupled systems, in order to minimize power consumption, VTT should be set close to 600mV.

Clock Data Recovery (CDR)

The CDR circuits for the four lanes of the high speed serial interface can be enabled through register 0x012 bits 3:0. For two-lane or one-lane operation, any of the two or any one lane can be chosen. Unused lanes, if enabled, will consume unnecessary power.

Logical Lane Mapping/Enabling

Each of the four physical high speed serial interface lanes, if used, must be mapped to an appropriate logical lane. For example, if four physical lanes are enabled for use with two converters then each of the four logical lanes are mapped to a distinct physical lane. Logical lanes 0, 1, 2 and 3 will contain IMSB, ILSB, QMSB, QLSB respectively. The logical lanes are enabled through register 0x17D and their mapping is controlled through register 0x016, as shown in **Table 11**.

Table 11. Logical lane mapping for JESD204A link

AD9128 configuration		Description	Reg. 0x017 D value
# of Lanes	# of DAC		
4	2	Each physical lane is mapped to a distinct logical lane	0x0F
2	2	Logical 0 should be mapped to the data I serial input and logical 2 to the data Q serial input. Logical lanes 3 and 4 are unused in this case	0x05
2	1	Logical 0 should be mapped to data MSBs and logical 2 to the data LSBs	0x05
1	2	Logical 0 should to be mapped to the one serial link and others are ignored	0x01
1	1	Logical 0 should both be mapped to the input lane carrying data	0x01

Each of the input lanes can be individually controlled as far as serial symbol mapping is concerned. Both the ordering of the bits (MSB to LSB or LSB to MSB) on bits 7:4, and the individual polarities on bits 3:0 are controlled through register 0x017.

A few mode bits are required in order to operate the non default mode of 4 Lanes or 2 Lanes and F = 1. These are contained in the Register 0x177. They enable sub-modes of the base configuration of the deframer:

- If F=2, Register 0x177 bits 5:2 must be set to 0111 (1 lane per DAC) and 0x176 must be set to 2.
- If F=4, Register 0x177 bits 5:2 must be set to 1011 (2 DACs 1 line) and 0x176 must be set to 4.
- If F=1, Register 0x177 bits 5:2 must be set to 0000

Programming the JESD204A link parameters

This section provides details of the link parameters with respect to the modes of operations supported by the AD9128. The link parameters are programmed through registers 0x150 to 0x15D. In order to achieve an accurate comparison, all the register values must be programmed the same at the transmitter and receiver end of the link.

1. 0x150: Provides the DID (Device ID or link ID). This is a comparison only value to identify the link name.
2. 0x151 bits 3:0: Provides the BID (Bank ID). It is an extension of the DID and meets the same requirements as the DID.
3. 0x152 bits 3:0: Provides the LID0 (lane ID for lane 0 within a link). The AD9128 will check the lane identification values on lane 0 only.
4. 0x153 bit7: Enables the scrambling function on the link.
5. 0x153 Bits4:0: Provides the number of lanes of the link associated with DID. This value L will be set based on the number of lanes used and is programmed as one less than

the number of lanes. The possible values for different DAC modes are:

- 4 Lanes, 2 DACs L=3
- 2 Lanes, 2 DACs L=1
- 1 Lane, 2 DACs L=0
- 2 Lanes, 1 DAC L=1
- 1 Lane, 1 DAC L=0

6. 0x154: Provides the F value or number of octets per frame per lane. Possible values for different modes are shown in Table 12.

Table 12. JESD204A link "F" value

AD9128 configuration		JESD204A F parameter	Register 0x0154 value
# of Lanes	# of DAC		
4	2	0	1
2	2	1	2
1	2	3	4
2	1	0	1
1	1	1	2

7. 0x155 bits4:0: Provide the K value (number of frames in a multiframe). This value is programmed at one less than the actual number. For the AD9128, the value can be:
   - K = 31 when F = 0 - 0x1F
   - K = 31 or 15 when F = 1 or 3- 0x1F or 0x0
8. 0x156: Provides the value of M (number of converters on the DAC used by the link). This value is programmed as one less than the actual number of converters.
   - 2 Converters – 0x01
   - 1 Converter – 0x00
   - 2 Lanes, 1 DAC HD = 1 (0x15A = 0x80
   - 1 Lane, 1 DAC HD = 0 (0x15A = 0x00)
9. 0x157 bits 7:6: Provide number of control words per frame. For the AD9128, this value is always 0 since it does not support control bits.
10. 0x157 bits 5:0: Represents the number of bits of resolution of the converter. It is programmed at one less than the actual value. The value is 0x0F for the AD9128.

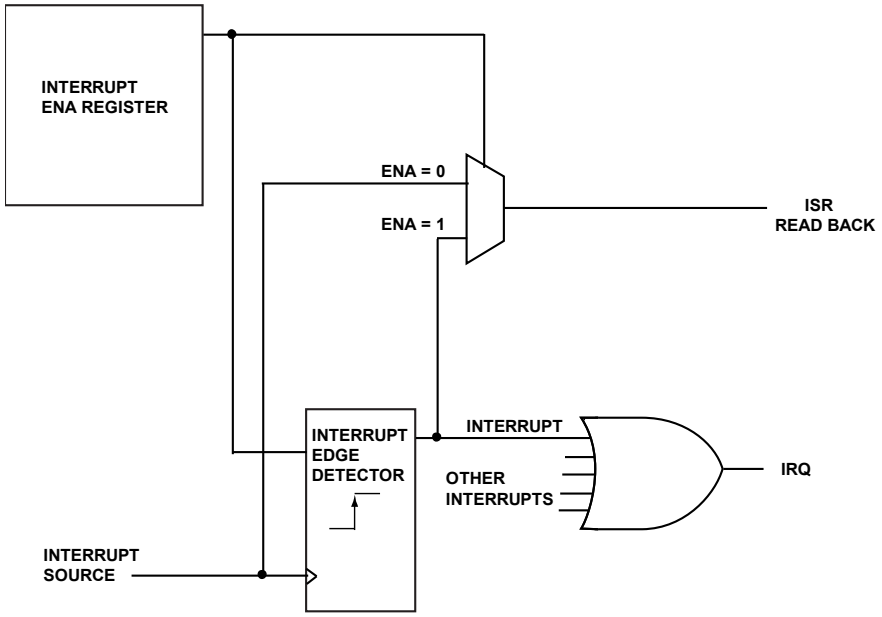


Figure 21. Interrupt control on the AD9128

11. 0x158 bits 5:0: Represents the number of bits in each sample being sent to the deframer. It is programmed at one less than the actual value. The value is 0x0F for the AD9128.
12. 0x159: Represents the number of samples per frame per converter and is programmed as one less than actual. The AD9128 supports only S = 1 (Reg. 0x159 set to 0).
13. 0x15A bit 7: Represents the high density HD parameter.
14. 0x15A bits 4:0: Represents CF (the number of control words per frame clock per lane). Possible values for register 0x15A are shown in Table 13.

Table 13. JESD204A link "HD" value

AD9128 configuration		JESD204A HD parameter	Register 0x015A value
# of Lanes	# of DAC		
4	2	1	0x80
2	2	0	0x00
1	2	0	0x00
2	1	1	0x80
1	1	0	0x00

15. 0x15B, 0x15C: Reserved fields. Should be set to 0 on both receiver and transmitter ends.
16. 0x15D: Checksum value equal to the sum of all the registers from 0x150 to 0x15C modulo 256.

Programming ILAS (Initial Lane Alignment Sequence) length:

In the AD9128 the length of the ILAS is programmed in register 0x178. It is programmed as the actual number of multi-frames times four (for a value of 1, the ILAS will be 4 multi-frames long). The AD9128 uses 8 multi-frames during the ILAS to accomplish multichip alignment (or 4 if multi-chip alignment is not needed).

In order to enable multichip alignment or latency locking, register 0x178 should be set to 0x02 and register 0x17B bit 0 should be set to 1. When latency locking/alignment is not needed in the system, register 0x178 should be set to 1 and 0x17B bit 0 to 0.

INTERRUPTS AND SYNCB CONTROL

The deframer monitors the link for errors, and in the AD9128 these errors can be reported back to the transmitter through different methods:

- Through interrupts
- Through the SYNCb signal as frame width assertion pulses on the line
- Through the SYNCb interface as forced SYNC requests.

Figure 27 shows a block diagram of the AD9128 interrupt control. Errors are counted on a lane by lane basis and either an error interrupt or a SYNCb event is triggered as the count reaches an Error Threshold. This threshold is programmed in Register 0x17C. Error counts for each lane can be monitored through the use of Registers 0x16D – 0x16F. The errors that the deframer will detect are: Bad Disparity Error, Not in Table Error, Unexpected control character, Alignment issue, Bad ILS Sequence, Configuration mismatch

The Interrupt request is masked by bits in registers 0x17A and 0x17B as follows:

0x17A, Bit7 – Bad Disparity (set high to trigger Interrupt request)
0x17A, Bit 6 – Not in Table
0x017A, Bit 5 – Unexpected control character
0x017A, Bit 4 – Interlane Alignment good
0x017A, Bit 3 – Good ILAS sequence
0x017A, Bit2 – Good Checksum
0x017A, Bit1 – Good Frame Sync
0x017A, Bit0 – Good Code Group Sync

The SYNCb frame width error reporting can be enabled by setting bit 1 of Register 0x175 high (Bad disparity, not in Table, and Unexpected control character will actuate this error reporting mode).

The SYNC force is masked by bits in 0x17B as follows:

0x17B, Bit7 – Bad disparity error (set high for error to force SYNCb high upon error threshold)
0x17B, Bit6 – Not in Table error
0x17B, Bit5 - Unexpected control character

ENABLING THE LINK

Once SYNCb setup/calibration is completed and clocks have settled, the link is ready to be established. The link can be established by setting bit 7 of Register 0x00A high. A startup sequence is performed for the delay path from DAC clock to SYNCb.

1. The SYNCb phase selector is reset to zero
2. The SYNCb FIFO is reset.
3. The previously programmed value of the SYNCb launch phase is programmed back to the SYNCb phase selector.

Once the startup sequence concludes inside the DAC, the SYNCb signal is allowed to fall. Conditional upon the link parameters being consistent at both ends and the DAC being able to capture data, the link will be established.

SERIAL PORT INTERFACE

Serial Port Operation

The serial port is a flexible, synchronous serial communications port allowing easy interface to many industry-standard micro-controllers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI® and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9128. Single or multiple byte transfers are supported, as well as MSB-first or LSB-first transfer formats. The serial interface ports can be configured as a single pin I/O (SDIO) or two unidirectional pins for input/output (SDIO/SDO).

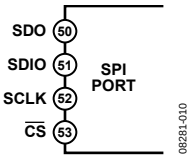


Figure 17. Serial Port Interface Pins

There are two phases to a communication cycle with the AD9128. Phase 1 is the instruction cycle (the writing of an instruction byte into the device), coincident with the first eight SCLK rising edges. The instruction byte provides the serial port controller with information regarding the data transfer cycle, Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is a read or write and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the device.

A logic high on the $\overline{CS}$ pin followed by a logic low resets the serial port timing to the initial state of the instruction cycle. From this state, the next eight rising SCLK edges represent the instruction bits of the current I/O operation.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the device and the system controller. Phase 2 of the communication cycle is a transfer of one or more data bytes. Registers change immediately upon writing to the last bit of each transfer byte, except for the frequency tuning word and NCO phase offsets that only change when the frequency update bit (Register 0x026, Bit 0) is set.

Table 14. Serial Port Instruction Byte

I7 (MSB)	I6	I5	I4	I3	I2	I1	I0 (LSB)
R/$\overline{W}$	A6	A5	A4	A3	A2	A1	A0

Data Format

The instruction byte contains the information shown in Table 14. R/$\overline{W}$, Bit 7 of the instruction byte determines whether a read or a write data transfer occurs after the instruction byte write. Logic 1 indicates a read operation, and Logic 0 indicates a write operation.

A6 to A0, Bit 6 to Bit 0 of the instruction byte, determine the register that is accessed during the data transfer portion of the communication cycle. For multibyte transfers, A6 is the starting byte address. The remaining register addresses are generated by the device based on the LSB_FIRST bit (Register 0x000, Bit 6).

SERIAL PORT PIN DESCRIPTIONS

Serial Clock (SCLK)

The serial clock pin synchronizes data to and from the device and runs the internal state machines. The maximum frequency of SCLK is 40 MHz. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

Chip Select ($\overline{CS}$)

An active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines. The SDO and SDIO pins go to a high impedance state when this input is high. During the communication cycle, chip select should stay low.

Serial Data I/O (SDIO)

Data is always written into the device on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Register 0x000, Bit 7. The default is Logic 0, configuring the SDIO pin as unidirectional.

Serial Data Out (SDO)

Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the device operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

Serial Port Options

The serial port can support both MSB-first and LSB-first data formats. This functionality is controlled by LSB_FIRST (Register 0x000, Bit 6). The default is MSB-first (LSB_FIRST = 0).

When LSB_FIRST = 0 (MSB-first), the instruction and data bit must be written from MSB to LSB. Multibyte data transfers in MSB-first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes should follow from the high address to low address. In MSB-first mode, the serial port internal byte address generator decrements for each data byte of the multibyte communication cycle.

When LSB_FIRST = 1 (LSB-first), the instruction and data bit must be written from LSB to MSB. Multibyte data transfers in LSB-first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The serial port internal byte address generator increments for each byte of the multibyte communication cycle.

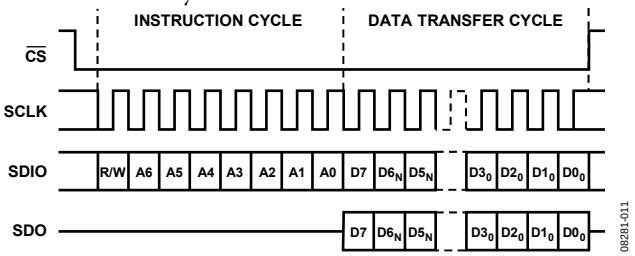


Figure 18. Serial Register Interface Timing MSB-First

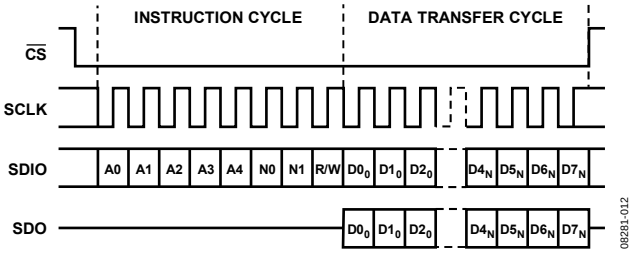


Figure 19. Serial Register Interface Timing LSB-First

The serial port controller data address decrements from the data address written toward 0x00 for multibyte I/O operations if the MSB-first mode is active. The serial port controller address increments from the data address written toward 0x7F for multibyte I/O operations if the LSB-first mode is active.

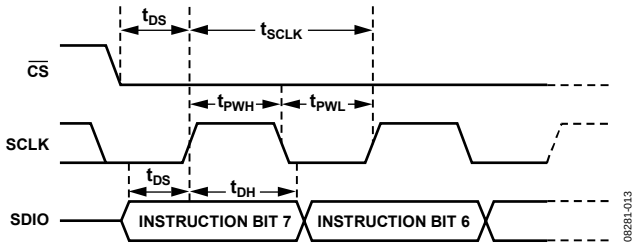


Figure 20. Timing Diagram for Serial Port Register Write

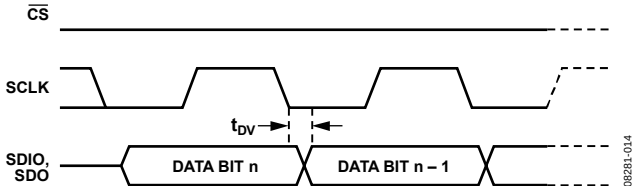


Figure 21. Timing Diagram for Serial Port Register Read

DIGITAL DATA PATH

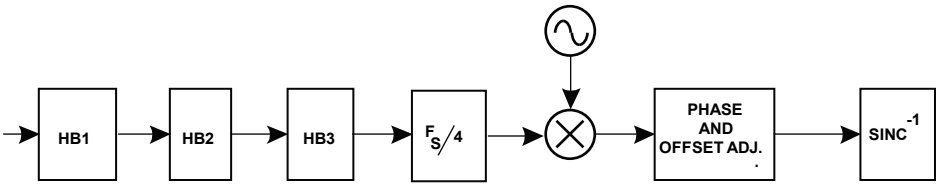


Figure 22 –Block Diagram of digital datapath

Figure 22 shows the functionality of the digital datapath. The digital processing includes three half-band interpolation filters, a quadrature modulator with a fine resolution NCO, Phase and Offset adjustment blocks and an inverse sinc filter.

The digital datapath accepts I and Q data streams and processes them as either two real data streams or as a quadrature data stream. To utilize any of the modulation modes, the data must be presented to the device in quadrature. The datapath can be used to process two independent real data streams with any of the interpolation modes. The coarse modulation (Fs/4) block can be used along with any of the interpolation filter modes.

INTERPOLATION FILTERS

The transmit path contains three interpolation filters. Each of the three interpolation filters provides a 2x increase in output data rate. The half-band (HB) filters can be cascaded or bypassed to provide 1x, 2x, 4x or 8x interpolation ratios. The bandwidth of the three half-band filters with respect to the data rate at the filter input is as follows:

- Bandwidth of HB1 = $0.8xf_{IN1}$
- Bandwidth of HB2 = $0.5xf_{IN2}$
- Bandwidth of HB3 = $0.4xf_{IN3}$

The usable bandwidth is defined as the frequency over which the filters have a passband ripple of less than +/-0.01dB and an image rejection of greater than 85dB.

The fine modulator performs frequency translation by performing a digital quadrature modulation of the input signal with a quadrature LO generated by the on-chip NCO.

1. 2x interpolation: Either the first (HB1) or second (HB2) half-band filter can be used for 2x interpolation (Register 0x00F). Figure 18 and Figure 19 show the frequency response when HB1 and HB2 are used respectively. The frequency (x-axis) is normalized to the DAC sample rate. Hence in this case, the bandwidth of HB1 is 0.4*Fdac or 0.8*Fdata. Similarly, the bandwidth of HB2 is 0.25*Fdac or 0.5*Fdata
2. 4x interpolation: It is accomplished using HB1 and HB2 (Register 0x00F). Note that it is not possible to use HB3 when in 4x interpolation mode. Figure 20 shows the frequency response for this case. The usable bandwidth is 0.2*Fdac or 0.8*Fdata.
3. 8x interpolation: In this case, all three filters are used. Figure 21 shows the frequency response for 8x interpolation. The usable bandwidth is 0.1*Fdac or 0.8*Fdata.

Table 15. AD9128 interpolation modes

Interpolation Mode	Filters used	Usable bandwidth
2x	HB1	(0.8 x Fdata) or (0.4 x Fdac)
	HB2	(0.5 x Fdata) or (0.25 x Fdac)
4x	HB1,2	(0.8 x Fdata) or (0.2 x Fdac)
8x	HB1,2,3	(0.8 x Fdata) or (0.1 x Fdac)

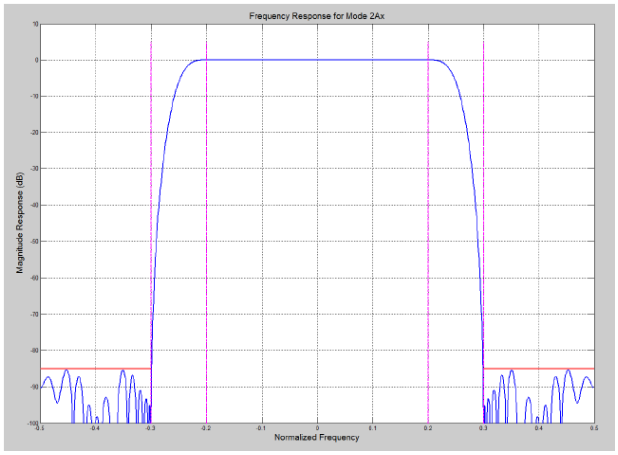


Figure 23. Transfer Function of HB1 in 2x interpolation mode. The frequency axis is normalized to the DAC sample rate.

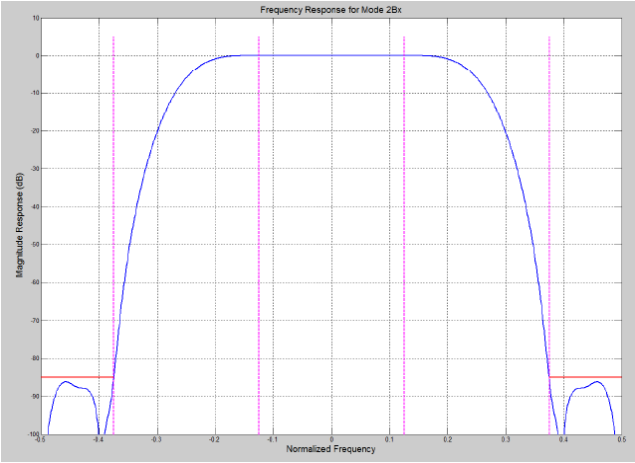


Figure 24 Transfer Function of HB2 in 2x interpolation mode. The frequency axis is normalized to the DAC sample rate.

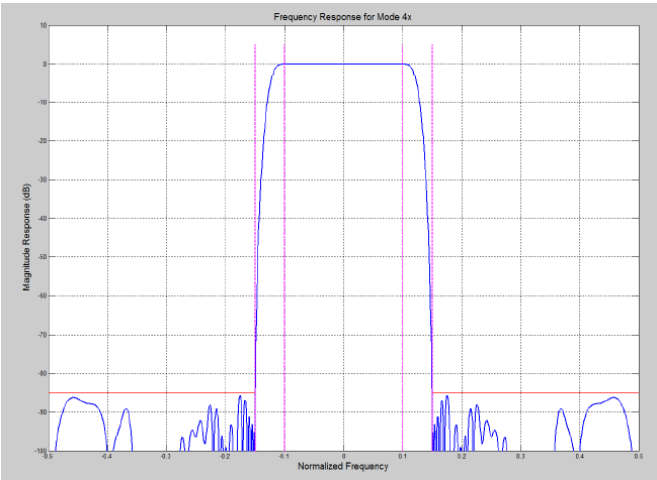


Figure 25 Transfer Function of HB1 and HB2 (cascaded) in 4x interpolation mode. The frequency axis is normalized to the DAC sample rate.

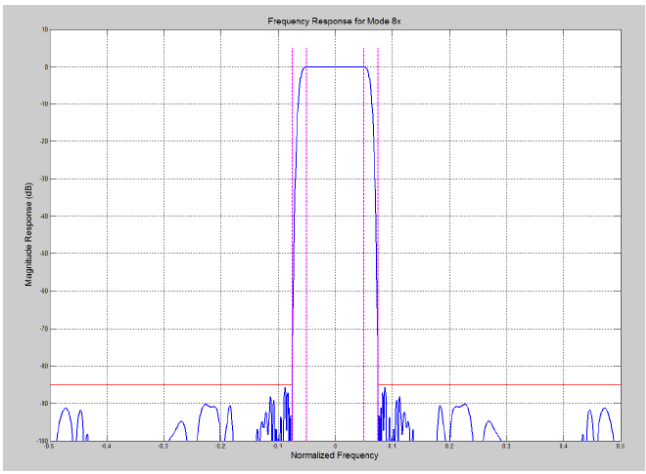


Figure 26 Transfer function of cascaded HB1, HB2 and HB3 in 8x interpolation mode

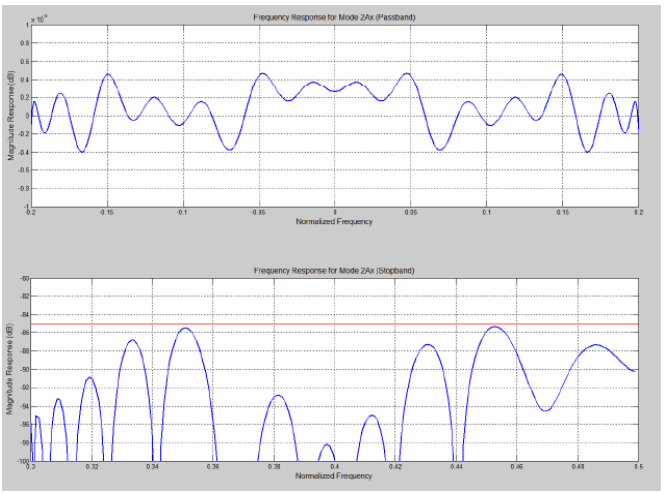


Figure 27 Pass band and stop-band characteristics of HB1. All three filters have pass-band ripple <0.01dB and image rejection > 85 dBc

FINE MODULATION

The fine modulation makes use of a numerically controlled oscillator, a phase shifter and a complex modulator to provide a means for modulating the signal by a programmable carrier signal. A block diagram of the fine modulator is shown in Figure 28. The fine modulator, in conjunction with the coarse modulator allows the signal to be placed anywhere in the output spectrum with very fine frequency resolution.

The quadrature modulator is used to mix the carrier signal generated by the NCO with the I and Q signals. The NCO produces a quadrature carrier signal to translate a single sideband of the input signal to a new center frequency. A complex carrier signal is a pair of sinusoidal waveforms of the same frequency, offset 90° from each other. The frequency of the complex carrier signal is set via the Frequency Tuning Word [31:0] value in Registers 0x020 thru 0x023.

The NCO operating frequency, f_{NCO}, is f_{DAC}. The frequency of the complex carrier signal can be set up to ½ f_{NCO} and is calculated as follows:

For $0 \le FTW \le 2^{31}$, $f_{Carrier} = \frac{FTW}{2^{32}} \times f_{DAC}$

For $2^{31} < FTW \le 2^{32}$, $f_{Carrier} = \left(1 - \frac{FTW}{2^{32}}\right) \times f_{DAC}$

Updating the Frequency Tuning Word

Unlike the other configuration registers, the frequency tuning word registers do not get updated immediately upon writing. After loading the FTW registers with the desired values, bit 0 of register 0x026 must transition from a 0 to a 1 for the new FTW to take effect.

Phase Offset Adjustment

A 16-bit phase offset may be added to the output of the phase accumulator via the serial port. This static phase adjustment results in an output signal that is offset by a constant angle relative to the nominal signal. This allows the user to phase align the NCO output with some external signal, if necessary. This can be especially useful when NCOs of multiple AD9128 devices are programmed for synchronization. The phase offset allows for the adjustment of the output timing between the devices. The static phase adjustment is sourced from the NCO Phase Offset Word [15:0] value located in Registers 0x024 and 0x025.

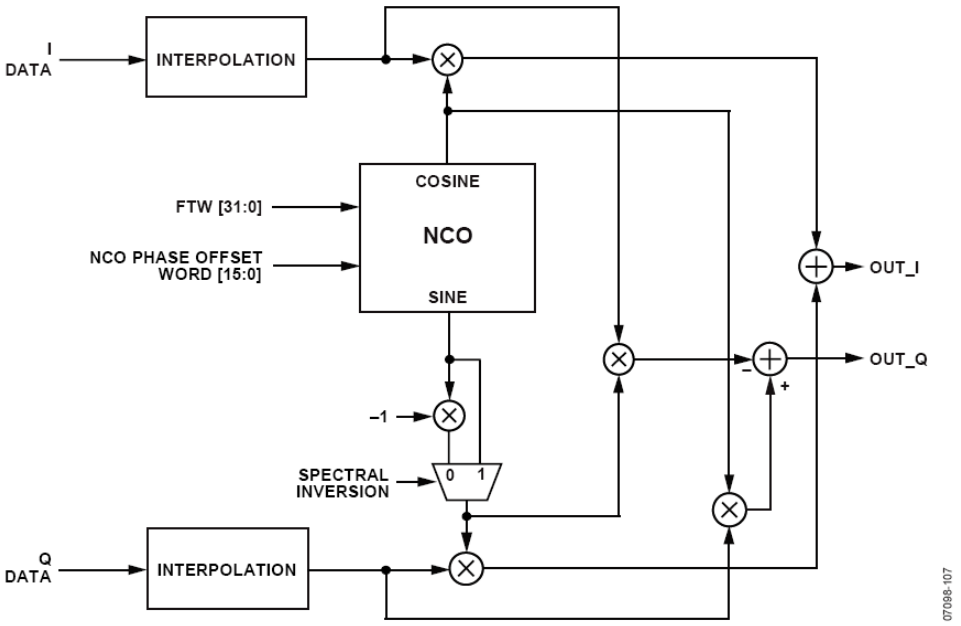


Figure 28 – Fine Modulator Block Diagram

COARSE MODULATION

The coarse modulation block at the end of the digital datapath provides a digital up-conversion of the incoming data by ¼ of its data rate (which is equal to Fdac, the DAC sampling rate). When a fixed up-conversion of Fs/4 is required, the NCO can be turned off and the coarse modulation block can be used. This will result in reduced power consumption. The setting for coarse modulation can be found in Register 0x00F, bit 4.

QUADRATURE PHASE CORRECTION

The purpose of the quadrature phase correction block is to enable compensation of the phase imbalance of the analog quadrature modulator following the DAC. If the quadrature

modulator has a phase imbalance, the unwanted sideband appears with significant energy. Tuning the Quadrature Phase Adjust value can optimize image rejection in single sideband radios.

Ordinarily, the I and Q channels have an angle of precisely 90° between them. The Quadrature Phase Adjustment is used to change the angle between the I and Q channels. When the I Phase Adj[9:0] is set to 1000000000b, the I DAC output moves approximately 1.75° away from the Q DAC output, creating an angle of 91.75° between the channels. When the I Phase Adj[9:0] is set to 0111111111b, the I DAC output moves approximately 1.75° towards the Q DAC output, creating an angle of 88.25° between the channels.

The Q Phase Adj[9:0] works in a similar fashion. When the Q Phase Adj[9:0] is set to 1000000000b, the Q DAC output moves approximately 1.75° away from the I DAC output, creating an angle of 91.75° between the channels. When the Q Phase Adj[9:0] is set to 0111111111b, the Q DAC output moves approximately 1.75° towards the I DAC output, creating an angle of 88.25° between the channels.

Based on these two endpoints, the combined resolution of the phase compensation register is approximately 7°/2048 or 0.00342° per code. The phase adjustment bits can be found in Registers 0x028 and 0x029.

DC OFFSET CORRECTION

The dc value of the I datapath and the Q datapath can be independently controlled by adjusting the I DAC Offset [15:0] and Q DAC Offset [15:0] values in Registers 0x02A thru 0x02B. These values are added directly to the datapath values. Care should be taken not to overrange the transmitted values.

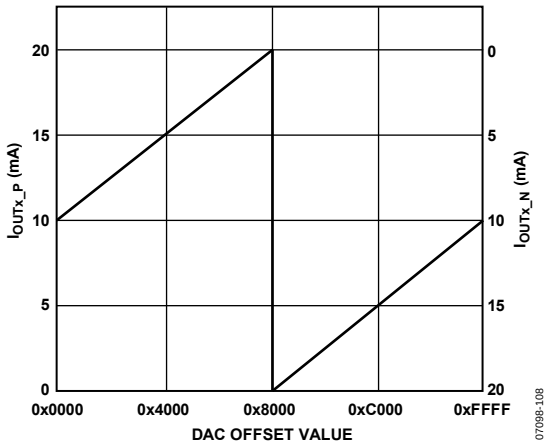


Figure 29. DAC Output Currents vs. DAC Offset Value

Figure 29 shows how the DAC offset current varies as a function of the I DAC Offset [15:0] and Q DAC Offset [15:0] values. With the digital inputs fixed at midscale (0x0000, twos complement data format), the figure shows the nominal I_{OUTP} and I_{OUTN} currents as the DAC offset value is swept from 0 to 65535. Because I_{OUTP} and I_{OUTN} are complementary current outputs, the sum of I_{OUTP} and I_{OUTN} is always 20 mA.

INVERSE SINC FILTER

The inverse sinc ($sinc^{-1}$) filter is a 9-tap FIR filter. The composite response of the $sinc^{-1}$ and the sin(x)/x response of the DAC is shown in Figure 30. The composite response has less than ±0.05 dB pass-band ripple up to a frequency of 0.4 × f_{DACCLK}. To provide the necessary peaking at the upper end of the pass band, the inverse sinc filters shown have an intrinsic insertion loss of about 3.2 dB.

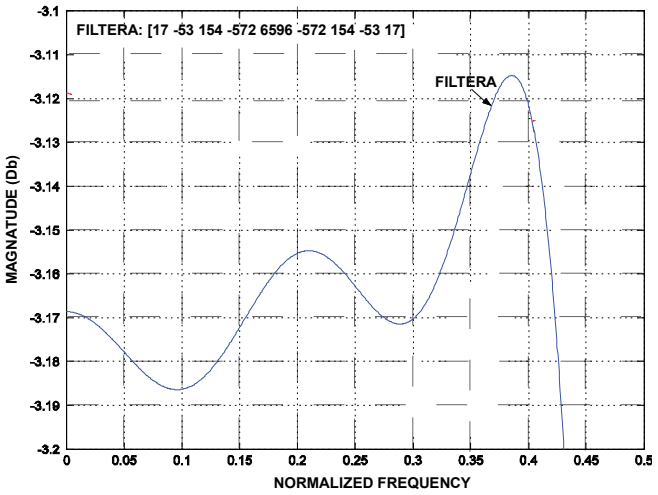


Figure 30. Sample composite responses of the $sinc^{-1}$ filter with sin(x)/x roll-off

DAC CLOCK CONFIGURATION

The AD9128 DAC sample clock (DACCLK) can be sourced directly or by clock multiplying. Clock multiplying employs the on-chip Phase Locked Loop (PLL) that accepts a reference clock operating at a sub-multiple of the desired DACCLK rate, most commonly the data input frequency. The PLL then multiplies the reference clock (REFCLK, provided through REFCLKP/N pins) up to the desired DACCLK frequency, which can then be used to generate all the internal clocks required by the DAC. The clock multiplier provides a high quality clock that meets the performance requirements of most applications. Using the on-chip clock multiplier removes the burden of generating and distributing the high speed DACCLK.

The second mode bypasses the clock multiplier circuitry and allows DACCLK to be sourced directly to the DAC core. This mode enables the user to source a very high quality clock directly to the DAC core. Sourcing the DACCLK directly through the DACCLKP, and DACCLKN pins may be necessary in demanding applications that require the lowest possible DAC output noise, particularly when directly synthesizing signals above 150 MHz.

Note that the AD9128 also requires a Frame clock (JESD_FRAMEP/N) that is used as the master clock for the serial interface. The REFCLK and DACCLK pins are dual-use pins: when not in use, they can be used for DAC alignment (DACALIGNP/N).

DRIVING THE DACCLK, REFCLK AND FRAME INPUTS

The REFCLK and DACCLK differential inputs share similar clock receiver input circuitry. Figure 31 shows a simplified circuit diagram of the input. The on-chip clock receiver has a differential input impedance of about 10 kΩ. It is self biased to a common-mode voltage of about 1.25 V (LVDS compliant). The inputs can be driven by direct coupling differential PECL or LVDS drivers. The inputs can also be ac-coupled if the driving source cannot meet the input compliance voltage of the receiver.

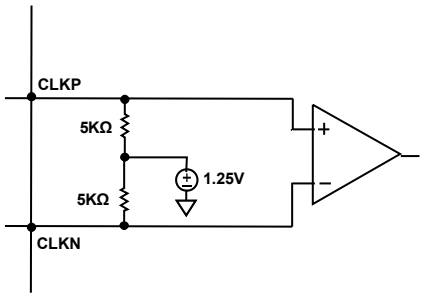


Figure 31. Clock Receiver input equivalent circuit.

If either REFCLKP/N or DACCLKP/N is used for the DACALIGN function, an external 100ohm resistor must be supplied between the two pins (DACALIGNP/DACALIGNN). The minimum input drive level to either of the clock inputs is 200 mV p-p differential. The optimal performance is achieved when the clock input signal is between 800 mV p-p differential and 1.6 V p-p differential. Whether using the on-chip clock multiplier or sourcing the DACCLK, directly, it is necessary that the input clock signal to the device has low jitter and fast edge rates to optimize the DAC noise performance.

DIRECT CLOCKING

Direct clocking with a low noise clock produces the lowest noise spectral density at the DAC outputs. To select the differential CLK inputs as the source for the DAC sampling clock, set the PLL enable bit (Register 0x018, Bit[7]) to 0. This powers down the internal PLL clock multiplier and selects the input from the DACCLKP and DACCLKN pins as the source for the internal DAC sample clock.

The device also has duty-cycle correction circuitry and differential input level correction circuitry. Enabling these circuits can provide improved performance in some cases. The control bits for these functions can be found in Register 0x019.

CLOCK MULTIPLICATION

The on-chip PLL clock multiplier circuit can be used to generate the DAC sample rate clock from a lower frequency reference clock. When the PLL enable bit (Register 0x018, Bit[7]) is set to 1, the clock multiplication circuit generates the DAC sample clock from the lower rate REFCLK input. The functional diagram of the clock multiplier is shown in Figure 32. The PLL can be setup and controlled through registers 0x018, 0x01A, and 0x01B.

The clock multiplication circuit operates such that the VCO outputs a frequency, f_{VCO}, equal to the REFCLK input signal frequency multiplied by N1 × N0.

$$f_{VCO} = f_{REFCLK} \times (N1 \times N0)$$

The DAC sample clock frequency, f_{DACCLK}, is equal to

$$f_{DACCLK} = f_{REFCLK} \times N1$$

The output frequency of the VCO must be chosen to keep f_{VCO} in the optimal operating range of 1.0 GHz to 2.1 GHz. The frequency of the reference clock and the values of N1 and N0 must be chosen so that the desired DACCLK frequency can be synthesized and the VCO output frequency is in the correct range.

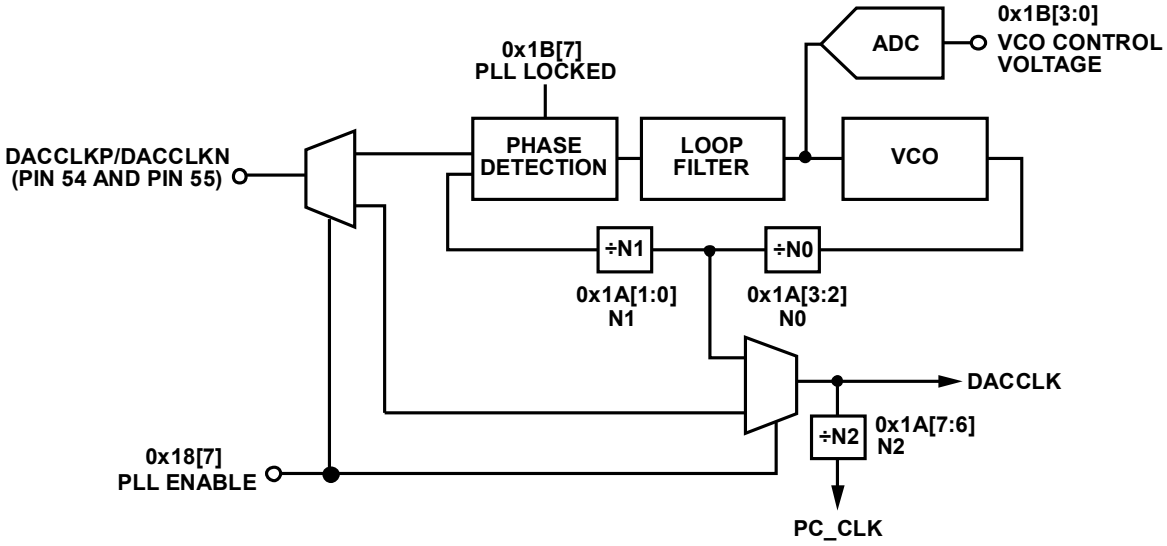


Figure 32. PLL Clock Multiplication Circuit

PLL SETTINGS

There are three settings for the PLL circuitry that should be programmed to their nominal values. The PLL values shown in **Table 16** are the recommended settings for these parameters.

Table 16. PLL Settings

PLL Parameter	Address		Optimal Setting
	Register	Bit	
PLL Loop Bandwidth [1:0]	0x077	[7:6]	11
PLL Charge Pump [4:0]Current	0x077	[4:0]	10001
PLL Cross Control Enable	0x01A	[4]	1

CONFIGURING THE VCO TUNING BAND

The PLL VCO has a valid operating range from approximately 1.0 GHz to 2.1 GHz covered in 63 overlapping frequency bands. For any desired VCO output frequency, there may be several valid PLL band select values. The frequency bands of a typical device are shown in **Error! Reference source not found.**. Device-to-device variations and operating temperature will affect the actual band frequency range. Therefore, it is required that the optimal PLL band select value be determined for each individual device.

Automatic VCO Band Select

The device has an automatic VCO band select feature on chip. Using the automatic VCO band select feature is a simple and reliable method of configuring the VCO frequency band. This feature is enabled by starting the PLL in manual mode, then placing the PLL in auto band select mode. This is done by setting Register 0x018 to a value of 0xCF, then to a value of 0xA0. When these values are written, the device executes an automated routine that determines the optimal VCO band setting for the device. The setting selected by the device ensures that the PLL remains locked over the full −40°C to +85°C operating temperature range of the device without further adjustment. (The PLL remains locked over the full temperature range even if the temperature during initialization is at one of the temperature extremes.)

ANALOG OUTPUTS

TRANSMIT DAC OPERATION

A simplified block diagram of the transmit path DACs is shown in *Figure 33*. The DAC core consists of a Current Source array, Switch Core, digital control logic, and full-scale output current control. The DAC full-scale output current (I_{OUTFS}) is nominally 20 mA. The output currents from the OUTP and OUTN pins are complementary, meaning that the sum of the two currents always equals the full-scale current of the DAC. The digital input code to the DAC determines the effective differential current delivered to the load.

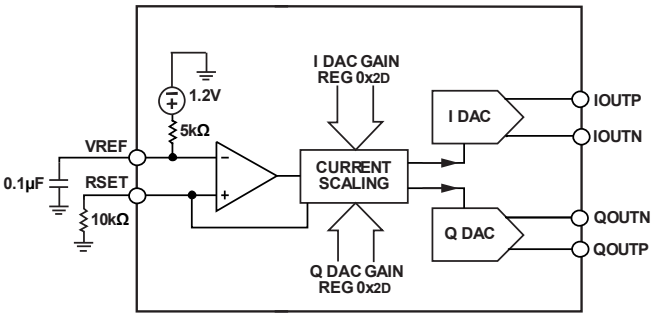


Figure 33. Simplified Block Diagram of DAC Core

The DAC has a 1.2V bandgap reference with an output impedance of 5 KΩ. The reference output voltage appears on the VREF pin. When using the internal reference, the VREF pin should be decoupled to AVSS with a 0.1µF capacitor. The internal reference should only be used for external circuits that draw DC currents of 2µA or less. For dynamic loads or static loads greater than 2µA, the VREF pin should be buffered. If desired, an external reference (between 1.10V and 1.30V) can be applied to the VREF pin. The internal reference can either be overdriven, or powered down by setting register 0x001 bit 5.

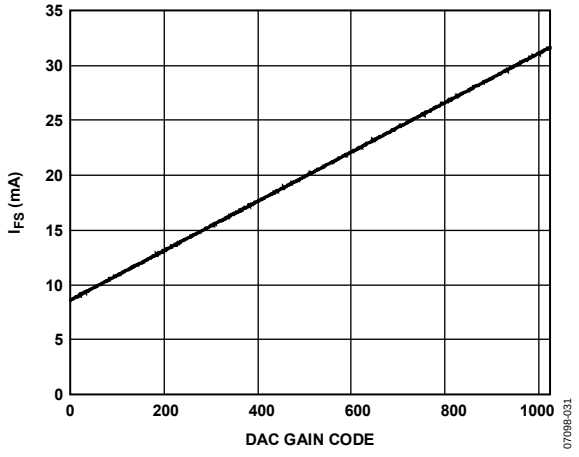


Figure 34. DAC Full-Scale Current vs. DAC Gain Code

For nominal values of VREF (1.2V), RSET (10 kΩ), and DAC Gain (512), the full-scale current of the DAC will be typically be 20.16 mA. The DAC full-scale current can be adjusted from 8.66mA to 31.66mA by setting the DAC Gain parameter setting as shown in *Figure 34*.

A 10 kΩ external resistor, R_{SET}, must be connected from the BIAS_RES pin to AVSS. This resistor, along with the reference control amplifier, sets up the correct internal bias currents for the DAC. Because the full-scale current is inversely proportional to this resistor, the tolerance of R_{SET} will be reflected in the full-scale output amplitude.

The equation for the full-scale current is shown below, where DAC gain is set individually for the I and Q DACs in registers 0x02D and 0x003, bit 0 respectively.

$$I_{FS} = \frac{V_{REF}}{R_{SET}} \times \left(72 + \left(\frac{3}{16} \times DAC\ gain\right)\right)$$

Transmit DAC Transfer Function

The output currents from the IOUT1P/2P and IOUT1N/2N pins are complementary, meaning that the sum of the two currents always equals the full-scale current of the DAC. The digital input code to the DAC determines the effective differential current delivered to the load. IOUT1P/2P provides maximum output current when all bits are high. The output currents versus DACCODE for the DAC outputs are expressed as:

$$I_{OUTP} = \left[\frac{DACCODE}{2^N}\right] \times I_{OUTFS} \quad (1)$$

$$I_{OUTN} = I_{OUTFS} - I_{OUTP} \quad (2)$$

where $DACCODE$ = 0 to $2^N - 1$.

Transmit DAC Output Configurations

The optimum noise and distortion performance of the AD9128 is realized when it is configured for differential operation. The common-mode error sources of the DAC outputs are significantly reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the frequency content of the reconstructed waveform increases and/or its amplitude increases. This is due to the first order cancellation of various dynamic common-mode distortion mechanisms, digital feed-through, and noise.

Figure 35 shows the most basic DAC output circuitry. A pair of resistors, R_O, is used to convert each of the complementary output currents to a differential voltage output, V_{OUT}. Because the current outputs of the DAC are high impedance, the differential driving point impedance of the DAC outputs, R_{OUT}, is equal to 2 × R_O. Figure 36 illustrates the output voltage waveforms.

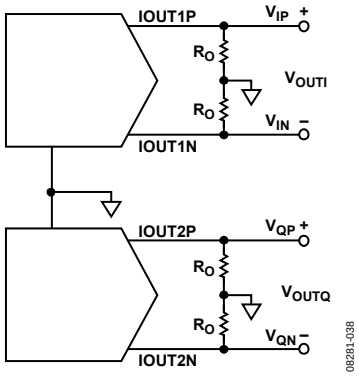


Figure 35. Basic Transmit DAC Output Circuit

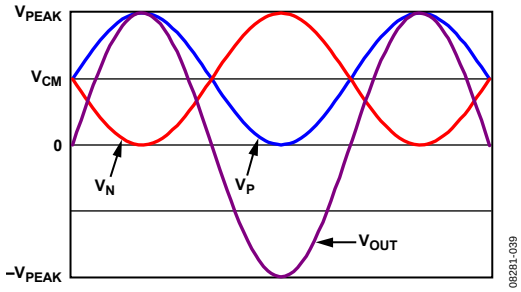


Figure 36. Voltage Output Waveforms

The common-mode signal voltage, V_{CM}, is calculated as;

$$V_{CM} = \frac{I_{FS}}{2} \times R_O$$

The peak output voltage, V_{PEAK}, is calculated as

$$V_{PEAK} = I_{FS} \times R_O$$

With this circuit configuration, the single-ended peak voltage is the same as the peak differential output voltage.

Transmit DAC Linear Output Signal Swing

To achieve optimum performance, the DAC outputs have a linear output compliance voltage range that must be adhered to. The linear output signal swing is dependent on the full-scale output current, I_{OUTFS}, and the common-mode level of the output. **Error! Reference source not found.** and **Error! Reference source not found.** show the IMD performance vs. the common-mode voltage at the different full-scale currents and output frequencies.

APPLICATIONS CIRCUITS

Interfacing to Modulators

The AD9128 interfaces to the ADL537x family of modulators with a minimal number of components. An example of the recommended interface circuitry is shown in Figure 37.

The baseband inputs of the ADL537x family require a dc bias of 500 mV. The nominal midscale output current on each output of the DAC is 10 mA (½ the full-scale current). Therefore, a single 50 Ω resistor to ground from each of the DAC outputs results in the desired 500 mV dc common-mode bias for the inputs to the ADL537x. The signal level can be reduced through the addition of the load resistor in parallel with the modulator inputs. The peak-to-peak voltage swing of the transmitted signal is

$$V_{SIGNAL} = I_{FS} \times \frac{[2 \times R_B \times R_L]}{[2 \times R_B + R_L]}$$

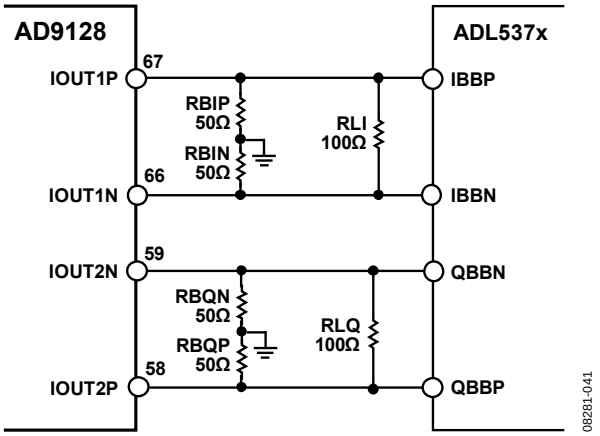


Figure 37. Typical Interface Circuitry Between the AD9128 and the ADL537x Family of Modulators

BASEBAND FILTER IMPLEMENTATION

Many applications require a baseband anti-imaging filter between the DAC and the modulator to filter out Nyquist images and broadband DAC noise. The filter can be inserted between the I-V resistors at the DAC output and the signal-level setting resistor across the modulator input. Doing this establishes the input and output impedances for the filter.

Figure 39 shows a fifth-order, low-pass filter. A common-mode choke is used between the I-V resistors and the remainder of the filter. This removes the common-mode signal produced by the DAC and prevents the common-mode signal from being converted to a differential signal, which can appear as unwanted spurious signals in the output spectrum. Splitting the first filter capacitor into two and grounding the center point creates a common-mode low-pass filter, providing additional common-mode rejection of high frequency signals. A purely differential filter can pass common-mode signals.

DRIVING THE ADL5375-15

The ADL5375-15 requires a 1500 mV dc bias and, therefore, requires a slightly more complex interface than most other Analog Devices, Inc, modulators. It is necessary to level shift the DAC output from a 500 mV dc bias to the 1500 mV dc bias that the ADL5375-15 requires. Level shifting can be achieved with a purely passive network, as shown in Figure 38. In this +network, the dc bias of the DAC remains at 500 mV while the input to the ADL5375-15 is 1500 mV. This passive, level shifting network introduces approximately 2 dB of loss in the ac signal.

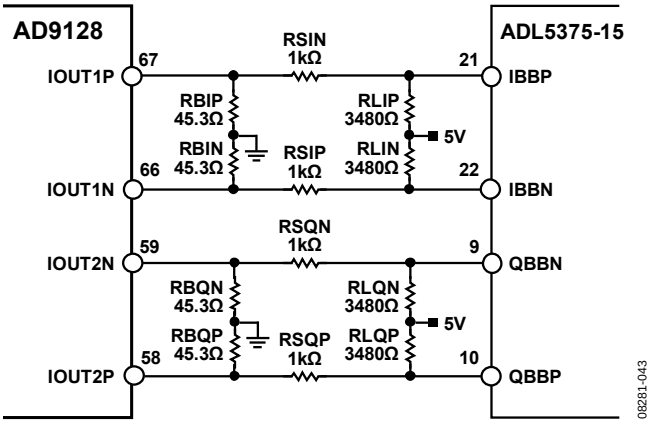


Figure 38. Passive, Level Shifting Network for Biasing ADL5375-15

REDUCING LO LEAKAGE AND UNWANTED SIDEBANDS

Analog quadrature modulators can introduce unwanted signals at the LO frequency due to dc offset voltages in the I and Q baseband inputs, as well as feedthrough paths from the LO input to the output. The LO feedthrough can be nulled by applying the correct dc offset voltages at the DAC output. This can be done using the by using the digital DC offset adjustments (Registers 0x02A and 0x02B).

Good sideband suppression requires both gain and phase matching of the I and Q signals. The I/Q phase adjust (Register 0x028 amd 0x029) and DAC FS adjust (Register 0x02D and Register 0x02F) registers can be used to calibrate I and Q transmit paths to optimize the sideband suppression.

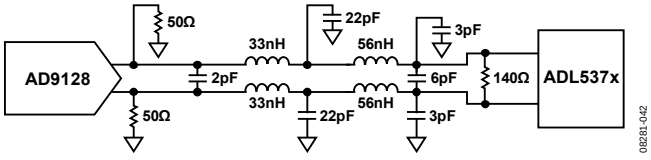


Figure 39. DAC Modulator Interface with Fifth-Order, Low Pass Filter

SERDES LINK PRINTED CIRCUIT BOARD DESIGN CONSIDERATIONS

MULTI-CHIP ALIGNMENT AND LATENCY LOCK

Note: If an internal frame clock signal is used, it is recommended that this configuration be setup prior to the configuration of the SERDES PLL.

This feature of the AD9128 enables multiple Dual DACs to be synchronized with each other. It also ensures a constant latency for each of the Dual DACs: in addition to all the DACs being synchronized, the latency of each DAC in the multi-chip system will be constant from link establishment to link establishment. In order to achieve this, the AD9128:

- Makes provision for an external alignment signal (DACALIGN) to be supplied to all the DACs
- Allows for the SYNCb launch timing of each of the DACs to be individually controlled. The SYNCb signal can be delayed by integral multiples of the frame clock signal. It can also be finely tuned using the SYNCb DLL. The SYNCb interface and usage models are described in detail later in this section.

EXTERNAL ALIGNMENT SIGNAL

In order to align multiple DACs to one another, an external differential DACALIGN edge may be required (see **SYNCb usage models** section). The alignment operation is done on a single edge of the differential DACALIGNP/N input. Note that DACALIGNP/N should be fed to the appropriate pins:

a. If DACCLKP/N is being used as the clock: DACALIGNP/N must be fed to the REFCLKP/N pins.
b. If the internal DAC PLL is being used to generate the clock: DACALIGNP/N must be fed to the DACCLKP/N pins.

In both cases, if DACALIGN is used, AC coupling cannot be employed. It should be an LVDS signal and a 100 ohm termination resistor should be placed between the pins used as DACALIGNP/N.

The external DACALIGN edge in conjunction with other internal clocks will be used to reset the interpolation clocks and the multi-frame counter of the DAC. The DACALIGN modes are controlled through register 0x00C. Bit 7 enables the use of the DACALIGN edge for DAC alignment. There are three possible scenarios in this case:

- The DACs can be aligned with the Frame clock. In this case, bit 5 of register 0x00C must be set. If set, the DACALIGN edge will be sampled by the next frame clock edge. The following rising edge of that frame clock will be sampled by the DAC clock and used as the alignment edge for the DAC reset.

  In order to ensure accurate alignment, a keep out window will exist between the DAC clock and the input Frame clock reference. This is required such that the same DAC clock samples the frame pulse on all DACs. A keep-out window will also exist between the Frame clock and the DACALIGN edge in order that the same Frame clock period is used by all DACs as a sampled alignment signal. (Keep-out specification TBD).
- The DACs can be aligned directly to the DACALIGN signal. In this case, bit 5 should not be set.
- In systems where external DACALIGN signal is not used, but the user would still like to align the DAC interpolation clocks to the reference/frame clock, bit 2 of register 0x00C must be set. In order for this mode to work, bit 5 of register 0x00C must be set high prior to setting bit 2. As with option 1, a keep out window will exist between the DAC clock and the input Frame clock reference.

SYNCB INTERFACE

The SYNCb interface is used to establish and communicate code group synchronization between the JESD204A deframer block and the transmitter (in accordance with the JESD204A specifications). The interface can be setup and monitored through registers 0x00A and 0x00B.

In order to enable multi-chip synchronization, the launch timing of the SYNCb signal can be either finely or coarsely controlled. If the user requires fine timing control of the SYNCb interface, the SYNCb DLL can be enabled through register 0x00B bit 7. The DLL locks on to the frame clock of the system (register 0x00B bit 6 can be read to check if the DLL has successfully locked). Note that if the internal DAC PLL is being used for the DAC clock, then the DLL should be enabled after a lock on the DAC PLL has been achieved (see section ***DAC Clock Configuration*** for details on DAC PLL).

The SYNCb delay offset can be manually set through register 0x00B bits 4:2 (see ***User Algorithm*** section below) or auto-calibrated by setting register 0x00A bit 4 high (see ***Automated Algorithm*** below).

User Algorithm

While the periodic SYNCb signal is being emitted, the FPGA can sweep the values to the SYNCB phase selector register (Reg 0x00B bit1:0 can be used to generate a periodic signal on SYNCb).

- The FPGA should be able to count the number of high and low captures on the periodic waveform with its FRAME clock. For instance, if register 0x00B bits1:0 are set to 11, there will be 4 high captures followed by 4 low captures.

- Consequently, the FPGA counter should expect 4 high and 4 low captures. When the SYNCb phase selection is changed and the FPGA counter deviates from a count of 4 (either 3 or 5 for one period f SYNCb oscillation), it implies that the SYNCb edge has passed over a FPGA frame clock boundary.
- The algorithm can then select a DLL phase 4 phases away from the phase producing the deviation. It is recommended that the DLL phase is the center of the capture eye.
- Also note that if the phase chosen is greater than the phase producing the deviation, then the user should apply a value of 1 to the Additional Latency Register (0x015). This is necessary in order to compensate for the extra delay in the chain produced by the SYNCb handoff to the FPGA.

Automated Algorithm

The AD9128 can also attempt to automatically find the center of the sampling eye. This can be done by setting bits 6 and 4 of register 0x00A. Note that the AD9128 must be programmed appropriately so that the data link can be successfully enabled.

- The automated algorithm will enable the link and capture the round trip delay from SYNCb to the data-path input of the DAC and record it.
- It will then sweep the phase selection for SYNCb launch backwards until the round trip delay changes. This is recorded as the first frame clock boundary of the FPGA.
- It will reset the phase selection to zero, calculate the round trip and sweep the phase selection forward until the round trip changes. This is recorded as the second frame clock boundary.
- It will then choose a phase halfway between the two edges, and record that value as the selected SYNCb phase. This phase will be readable through the register 0x00B bits 4:2 as long as bit 4 of Register 0x00A remains set.

SYNCB USAGE MODELS

The SYNCb setup for multi-chip synchronization can be handled in 2 ways:

SPI interface

This option is possible only when the DACs establish their own individual link with a common external frame clock (SYNCb signals are not combined at the transmitter). This scenario is depicted in Figure 38.If each DAC exists on its own JESD204A link within the system, there exists no path for communication between the DACs since the SYNCb signals are sent individually to the transmitter. If one lane loses lock, only that transmit link is compromised. SPI based synchronization is sufficient and can be accomplished through setting bits 2 and 5 of register 0x00C (bit 4 optional). The Align to frame request (Register 0x00C, bit 2) will allow the internal SYNCb FIFO reset to be determinant and guarantees the same forward path latency on each of the independent links.

External alignment signal (DACALIGN)

a. If user supplies external frame clock:

If the SYNCb signals from the DACs are combined at the transmitter, then an external alignment (DACALIGN) signal is needed for all the DACs. Bits 5 and 7 of register 0x00C must be set high (bits 6 and 4 optional) in this case bit 2. This will ensure that the multi-chip alignment is based on the frame source clock. This scenario is depicted in Figure 41.

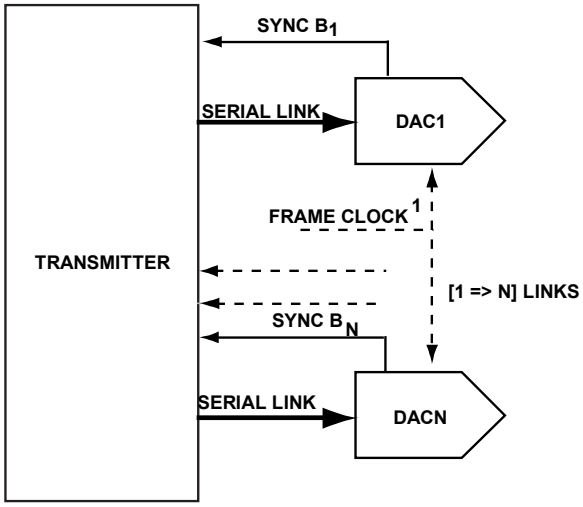


Figure 40.Multichip operation when each DAC operates with an independent autonomous link

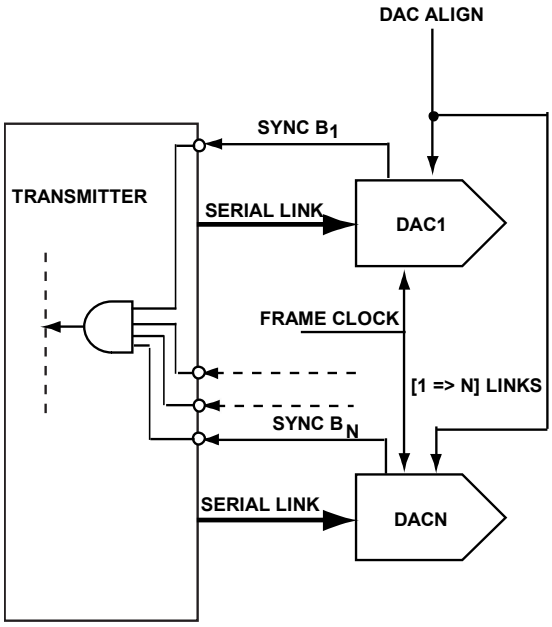


Figure 41. Mult-chip synchronization with external DACALIGN signal when SYNCb is combined at the transmitter

b. If internal frame clock is used:

If user supplies DAC clock only and no frame clock (frame clock generated internally in the DAC), then DACALIGN signal must be applied to all the DACs with Register 0x00C set to 0xD0. The internal frame clock should also be locked to the internal data rate clock (Register 0x01D set to 0x30). Note that calibration of the SYNCb interface must be performed after the DACALIGN signal is applied.

In addition to setting the modes of operation for the Multichip alignment, the value of the transmitter's latency should be written into register 0x014 bits 4:0. This latency is measured in frame clock periods through the transmitter from SYNCb capture to the time when the first ILAS symbol leaves the transmitter. This value, typically a fractional number of frame clock periods, should be rounded to the nearest whole number of frame clock cycles. If the TX latency is not known, a diagnostic mode can be used to find this value:

- Set Register 0x013 bit 5 high for each DAC in the system
- The additional latency to be used is generated in Register 0x015 bits 4:0 after the link is established.
- The average additional latency (for all DACs) generated by this mode should be used as the common TX latency for all DACs

When (re)alignment is required, DACALIGN signal must be transitioned to its pre-alignment value (default: low) and set (default: high) again. Using the above methods for multi-chip alignment will ensure that the latency of the forward path will remain constant from link establishment to link establishment. The only exception could occur if the DAC experiences a power glitch.

AD9128 STARTUP SEQUENCE AND LATENCY ALIGNMENT PROCEDURE

This section describes the recommended start-up sequence for the AD9128. And presents two alternative sequences for performing deterministic latency alignment among two or more AD9128 devices.

STARTUP FLOWCHART

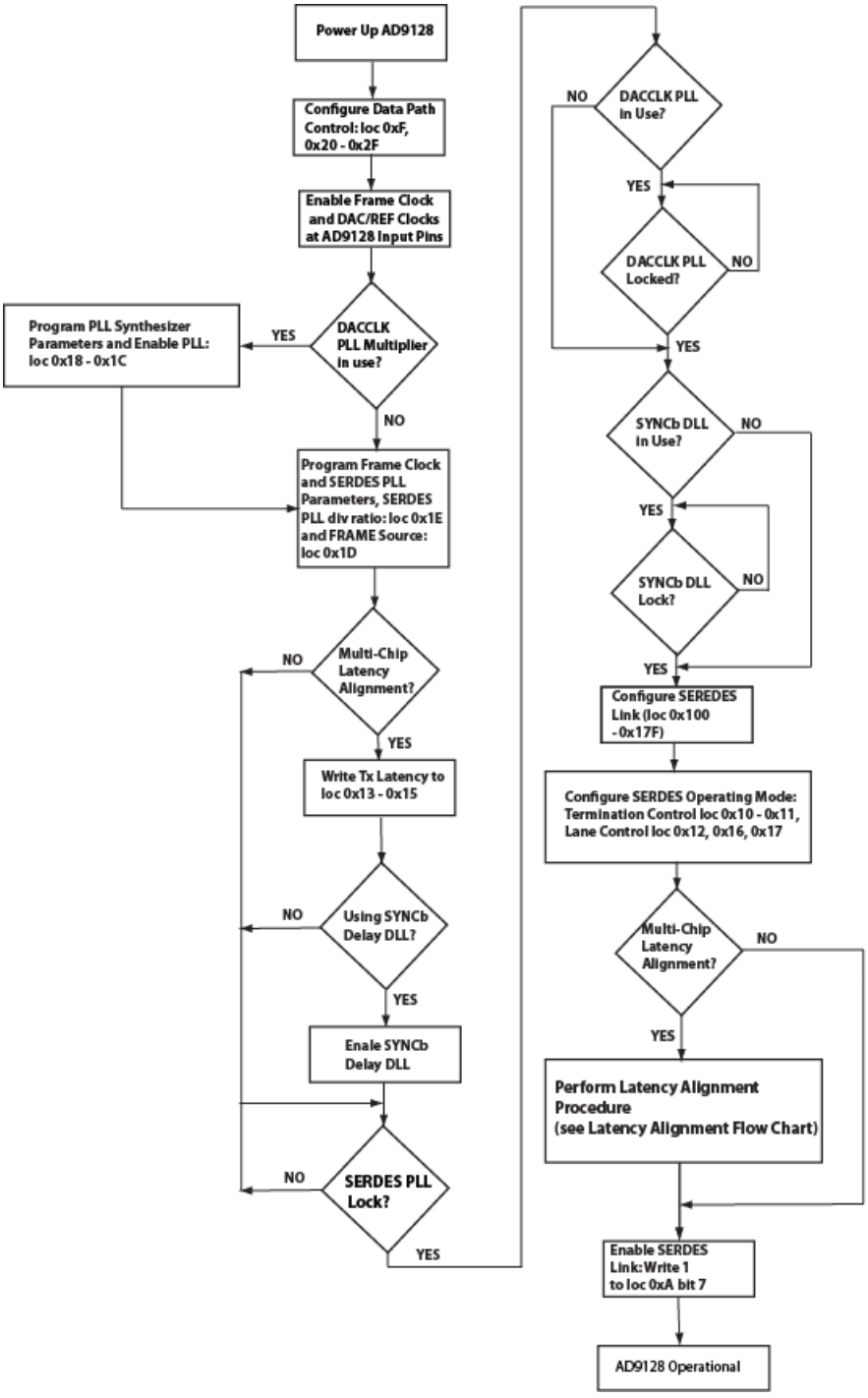


Figure 42. Start-up sequence Flow Chart for the AD9128

MULTI-CHIP LATENCY ALIGNMENT FLOWCHART

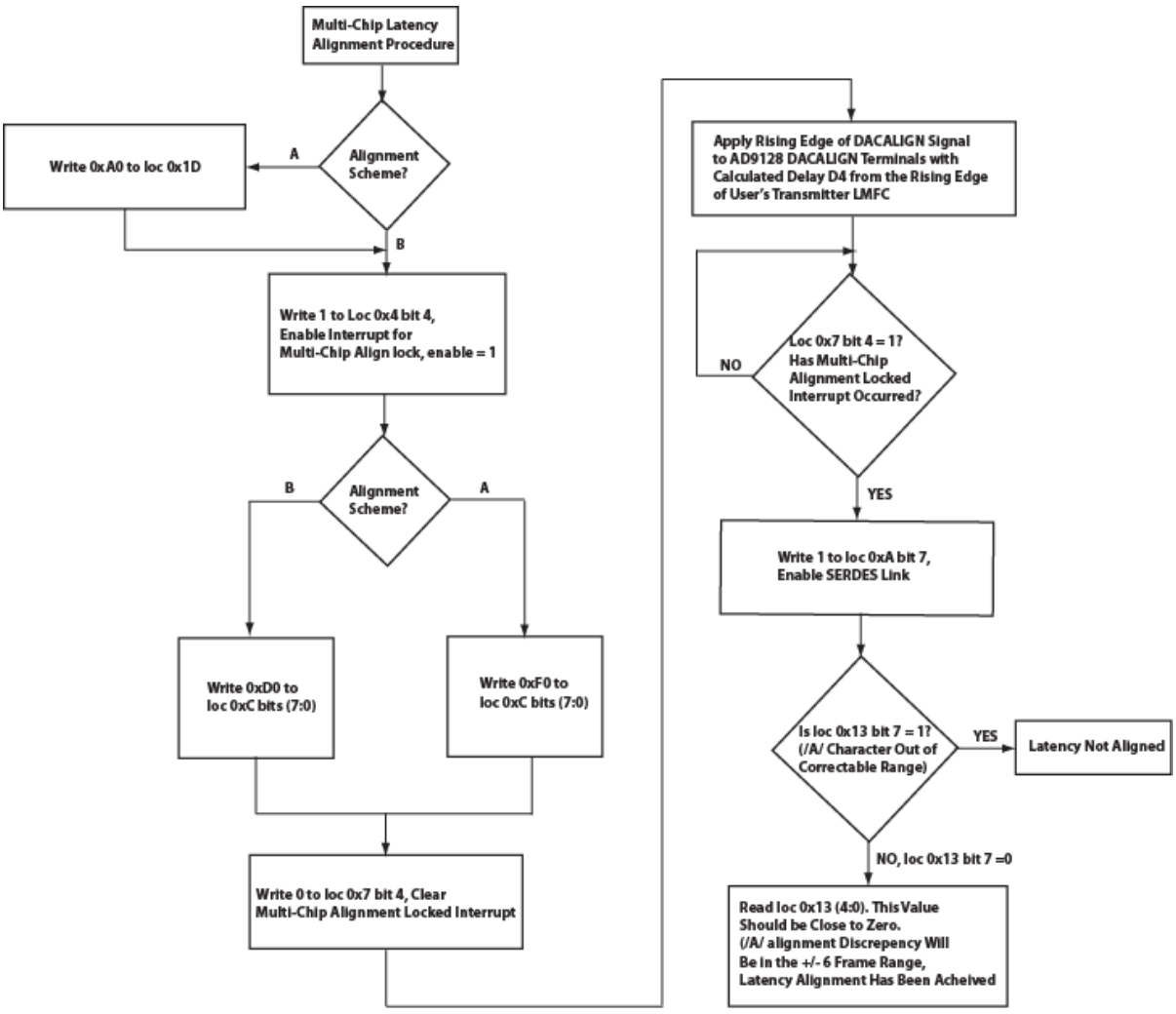


Figure 43. . Multi-Chip Latency Alignment Flow Chart for the AD9128

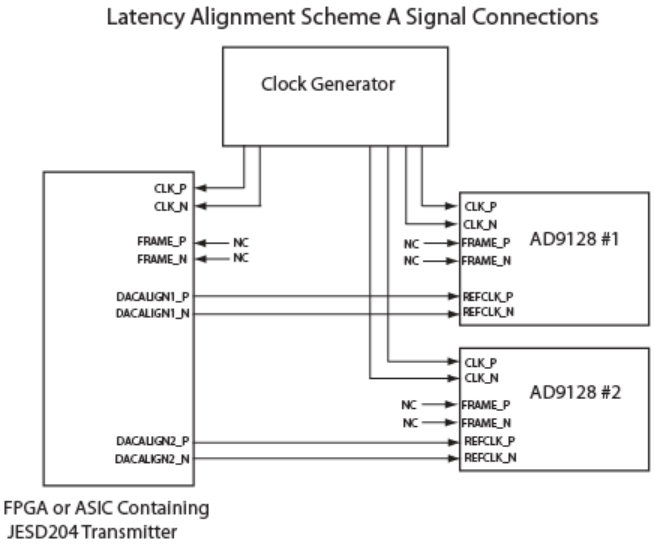


Figure 44. Latency Alignment Scheme A

In latency alignment scheme A, the DACALIGN signal from the JESD204 transmitter tells each AD9128 which edge of the DAC sampling clock to use to reset it's LMFC (local multiframe counter).

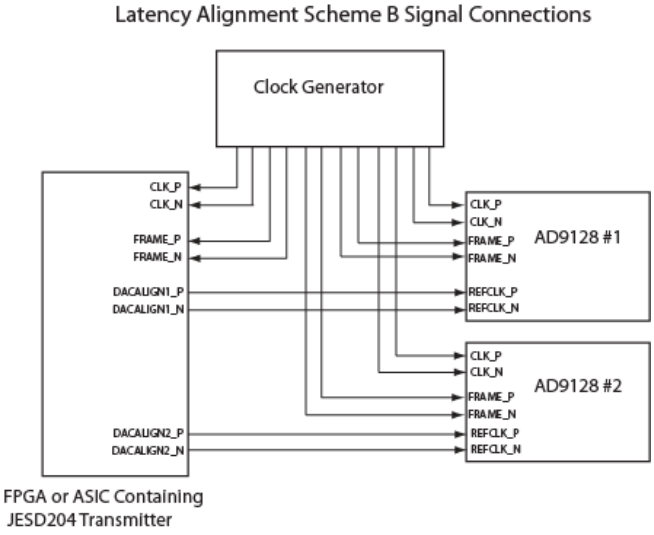


Figure 45. Latency Alignment Scheme B

In latency alignment scheme B, the DACLIGN signal from the JESD204 transmitter tells each AD9128 which edge of FRAME_P/FRAME_N to use to reset each AD9128's LMFC.

Transmitter Setup for AD9128 Latency Alignment

- The Transmitter Calculates D4.
- D4 is the delay from the rising edge of the LMFC cycle to the rising edge of the DACALIGN signal sent from the transmitter to the receiver.

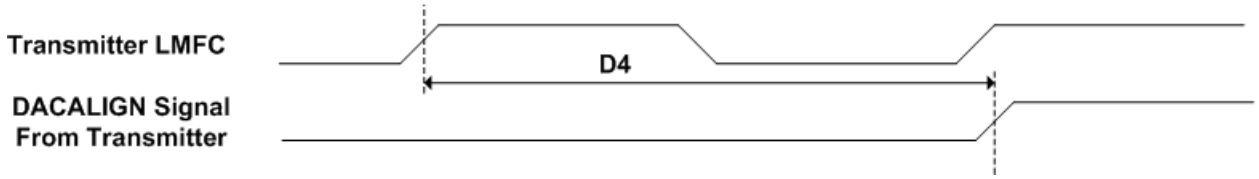
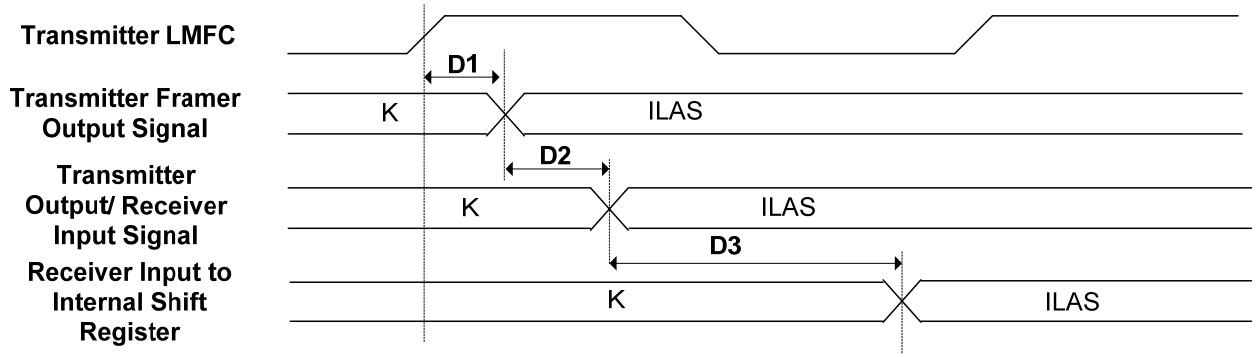


Figure 46. DACALIGN Transmitter Output and Transmitter LMFC Timing



D1 = Delay from LMFC rising edge to ILAS start at Tx Framer output

D2 = Delay from Transmitter Framer output to Transmitter Output
D3 = Delay from Receiver Input to Internal Shift Register (Receiver Latency),
D3 = 34 in AD9128

The unit of Delay is Samples. In HuaWei's system 1 Frame = 1 Sample = 1 Byte

Calculations:
X = D1 + D2 + D3 = D1 + D2 + 34
Y = X MOD 32
D4 = 32 - Y

ILAS: Inter-Lane Alignment Sequence
LMFC: Local Multi-Frame Clock

Figure 47. Calculating the D4 Delay Time

TESTING THE SERDES LINK AT THE BOARD LEVEL

REGISTER MAP

Register name	*Address*	*Bit7*	*Bit6*	*Bit5*	*Bit4*	*Bit3*	*Bit2*	*Bit1*	*Bit0*	*Default*
Comm	0x00		LSB first	Soft Reset	Long Mode					0x10
PowerControl	0x01	Pwr Down DAC I	Pwr Down DAC Q	Pwr Down Voltage Ref				Pwr Down clock receiver	Txen from SPI	0x11
SERDES SPI status	0x02		Deframer Interrupt	Link Established		Alignment character out of range	SYNCb auto cal done	Syncb autocal failed	Deframer SPI Ready	0x00
Data Format	0x03	Binary Enable					Poll Interuptb	Single DAC	I/Q DAC Select	0x00
IntEna0	0x04	Enable DAC PLL LockLost	Enable DAC PLL Locked	Enable link established	Enable link dropped	Enable syncb autocal fail	Enable syncb autocal done	Enable Fifo Warn1	Enable Fifo Warn2	0x00
IntEna1	0x05				Enable AED Pass	Enable AED Fail	Enable SED Fail			0x00
IntEna2	0x06	Enable SERDES PLL LockLost	Enable SERDES PLL Locked	Enable Serdes FIFO warn		Enable A character out of range		Enable BER finished	Enable BER count max	0x00
IntSrv0	0x07	DAC PLL LockLost	DAC PLL Locked	Link established	Link dropped	Syncb autocal fail	Syncb autocal done	Fifo Warn1	Fifo Warn2	0x00
IntSrv1	0x08				AED Pass IRQ	AED Fail IRQ	SED Fail IRQ			0x00
IntSrv2	0x09	SERDES PLL LockLost	SERDES PLL Locked	Serdes FIFO warn		A character out of range		BER finished	BER count max	0x00
Syncb/Link Control	0x0A	Enable Serial Link	Delay SYNCb	SYNCb Polarity	Autocal SYNCb delay	Release lock on data path in man mode	Enable SYNCb 1	Enable SYNCb 2	Enable SYNCb Input	0x64
Syncb delay control	0x0B	Enable SYNCb DLL	SYNCb DLL Lock	SYNCb launch from frame falling edge	Syncb delay offset[2:0]			Syncb Timing Testmode[1:0]		0x00
Align Control[1]	0x0C	Enable DACAlign Buffer	Use Rising Edge DACAlign	Align based on Frame Reference	Align input sampled by DACCLK rising	Enable Align Machine	Align to Frame Request	Arm One Shot	One Shot Tripped	0x50

[1] Align Machine (0x0C[3]) must be enabled before writing to this register.

Register name	*Address*	*Bit7*	*Bit6*	*Bit5*	*Bit4*	*Bit3*	*Bit2*	*Bit1*	*Bit0*	*Default*
					edge					
Align Control	0x0D	SYNCb reset FIFO warn	SYNCb Fifo depth[1:0]			SYNCb value at pin	DAC phase adjustment[2:0]			0x00
Align Status	0x0E	Align Status[7:0]								-
DataPath CTRL	0x0F	Set to make release of data force manual	Bypass InvSinc	Bypass Phase, Digital Gain, and Offset Adjustment	Bypass fs/4 Moduluation	Filter and NCO Mode Control [3:0]				0x70
Termination control	0x10			Enable Rcal	Enable Vtt buffer	Vtt buffer ctrl[3:0]				0x20
RCAL Force	0x11				Force rcal	Rcal value[3:0]				0x00
Lane power Control	0x12	SERDES output lane matrix[1:0]				Phy Lane enable[3:0]				0x4F
"A" Alignment Status	0x13			Enable Auto Calc	Discrepancy[4:0]					0x00
Latency Reg1	0x14				TX Latency[4:0]					0x00
Latency Reg2	0x15				Additional Latency[4:0]					0x00
Xbar support	0x16	SERDES Input Lane Matrix[7:0]								0xe4
Xbar support	0x17	SERDES symbol reverse[7:4]				SERDES symbol bit invert[3:0]				0x00
PLL Control	0x18	Enable PLL	Enable Pll Manual	Manual Band[5:0]						0x40
Clk Receiver Control	0x19	DAC Clk Duty Correction	Ref Clk Duty Correction	DAC Clk Cross Correction	REF Clk Cross Correction	Manual Cross Sign	Manual Cross Amplitude[2:0]			0x3F
PLL Control	0x1A	Divider 2[1:0]			Enable PLL Cross Ctrl	Divider 0[1:0]		Divider 1[1:0]		0xD9
PLL Status	0x1B	PLL Lock				PLL ADC Control Voltage[3:0]				-
PLL Status	0x1C			PLL Band[5:0]						-
SERDES PLL control	0x1D	Powerdown frame input buffer	Frame source reference input	Frame source internal	Frame locked to datarate counter					0x00
SERDES PLL	0x1E	Override SERDES	Serdes PLL Lock	Override SERDES	Power Down	SERDES pclk div[3:0]				0x01

Register name	*Address*	*Bit7*	*Bit6*	*Bit5*	*Bit4*	*Bit3*	*Bit2*	*Bit1*	*Bit0*	*Default*
Config		DLL lock		PLL Lock	SERDES PLL					
CHIP ID	0x1F	Chip ID[7:0]								0x09
FTW low	0x20	FTW[7:0]								0x00
FTW mid low	0x21	FTW[15:8]								0x00
FTW mid high	0x22	FTW[23:16]								0x00
FTW high	0x23	FTW[31:24]								0x00
NCO Phase low	0x24	NCO Phase Offset[7:0]								0x00
NCO Phase high	0x25	NCO Phase Offset[15:8]								0x00
NCO Updating	0x26								SPI FTW Update	0x00
Registers 0x28-0x2F control both I and Q DACs. Setting register 0x03[0]=0 selects the I DAC. Setting register 0x03[0]=1 selects the Q DAC.										
Phase Word low	0x28	I/Q PhaseWord[7:0]								0x00
Phase Word high	0x29					I/Q PhaseWord[11:8]				0x00
DC Offset low	0x2A	I/Q DC Offset[7:0]								0x00
DC Offset high	0x2B	I/Q DC Offset[15:8]								0x00
DC Gain	0x2C	I/Q Digital Gain[7:0]								0x40
DAC Gain Adj	0x2D	I/Q DAC Analog Full Scale Adjust[7:0]								0xF9
Reserved	0x2E	RESERVED								0x00
DAC Gain Adj	0x2F				I/Q DAC Analog Full Scale Adjust [9:8]					0x08
BER tester control	0x30	Enable BER	BER cont		BER period select[4:0]					0x00
BER count LSBs	0x31	BER count[7:0]								-
BER count MSBs	0x32	BER count[15:8]								-
TX enable Control	0x33	PD Voltage Ref	PD Clocks	PD DACs	PD CDRs	PD Deframer	PD DAC Datapath	Extend risng edge of TXen	Txen rising edge extend length	0x00
Sample test control	0x34							Sample test error	Sample test mode	0x00

Register name	*Address*	*Bit7*	*Bit6*	*Bit5*	*Bit4*	*Bit3*	*Bit2*	*Bit1*	*Bit0*	*Default*
Deframer wrapper control	0x35						Syncb FIFO reset		Deframer FIFO reset	0x00
Deframer wrapper FIFOs full/empty status	0x36	Deframer FIFO Full[3:0]				Deframer FIFO Empty[3:0]				-
Equalization	0x3B					hrx cdr eq[3:0]				0x0F
SERDES PRBS control	0x3D	Enable PRBS error output	PRBS lane select[1:0]		Enable PRBS	PRBS hold pattern	PRBS select mode[1:0]			0x00
FIFO Therm	0x40	FIFO Phase Thermometer[7:0]								-
Datapath FIFO control	0x41	SPI based FIFO write side reset	SPI based FIFO align ack	FIFO force data testmode			FIFO WrPhaseSet[2:0]			0x04
Latency measurement compare value	0x42	Latency compare value[7:0]								0x00
Latency measurement compare value	0x43	Latency compare value[15:0]								0x00
LMFC Compare Value	0x44	LMFC at compare point[7:0]								-
NCO Reset	0x45							NCO reset occurred	Arm NCO Reset	0x00
NCO Reset	0x46	I compare value for NCO reset[7:0]								0x00
NCO Reset	0x47	I compare value for NCO reset[15:0]								0x00
NCO Reset	0x48	Q compare value for NCO reset[7:0]								0x00
NCO Reset	0x49	Q compare value for NCO reset[15:0]								0x00
SED Ctrl	0x63	Enable SED		SED Fail		Enable AED		AED Fail	AED Pass	0x00
SED1l	0x64	Sample Error Detect Pattern 1[7:0]								0x00
SED1h	0x65	Sample Error Detect Pattern 1[15:8]								0x00
SED2l	0x66	Sample Error Detect Pattern 2[7:0]								0x00

Register name	*Address*	*Bit7*	*Bit6*	*Bit5*	*Bit4*	*Bit3*	*Bit2*	*Bit1*	*Bit0*	*Default*
SED2h	0x67	Sample Error Detect Pattern 2[15:8]								0x00
SED3l	0x68	Sample Error Detect Pattern 3[7:0]								0x00
SED3h	0x69	Sample Error Detect Pattern 3[15:8]								0x00
SED4l	0x6A	Sample Error Detect Pattern 4[7:0]								0x00
SED4h	0x6B	Sample Error Detect Pattern 4[15:8]								0x00
SEDRl	0x6C	Sample Error Detect Status I[7:0]								0x00
SEDRh	0x6D	Sample Error Detect Status I[15:8]								0x00
SEDFl	0x6E	Sample Error Detect Status Q[7:0]								0x00
SEDFh	0x6F	Sample Error Detect Status Q[15:8]								0x00
PLL Control #1	0x77	PLL Loop Filter[1:0]			PLL Charge Pump Multiplier[1:0]		PLL Charge Pump Nominal Current[2:0]			0xD1
PLL Control #2	0x7B	PFD Pulse Width[1:0]		VCO Amplitude Control[1:0]		VCO Bias Control[1:0]		VCO Gate Bias[1:0]		0xD7
Register 0x100-0x1F7 can only be accessed when the SerDes PLL is locked. Check register 0x02[0] for the deframer register status.										
Registers 0x100-0x126 are read only values transmitted during ILAS.										
did reg	0x100	DID READ[7:0]								-
bid reg	0x101					BID READ[3:0]				-
lid reg	0x102				LID READ[4:0]					-
scr l reg	0x103	SCR READ			L READ[4:0]					-
f reg	0x104	F READ[7:0]								-
k reg	0x105				K READ[4:0]					-
m reg	0x106	M READ[7:0]								-
cs n reg	0x107	CS READ[1:0]			N READ[4:0]					-
np reg	0x108				NP READ[4:0]					-
s reg	0x109				S READ[4:0]					-
hd cf reg	0x10A	HD READ			CF READ[4:0]					-
res1 reg	0x10B	RES1 READ[7:0]								-
res2 reg	0x10C	RES2 READ[7:0]								-
checksum 0 reg	0x10D	FCHK0 READ[7:0]								-

Register name	*Address*	*Bit7*	*Bit6*	*Bit5*	*Bit4*	*Bit3*	*Bit2*	*Bit1*	*Bit0*	*Default*
compsum 0 reg	0x10E	FCMP0 READ[7:0]								-
lid1 reg	0x112				LID1 READ[4:0]					-
checksum 1 reg	0x115	FCHK1 READ[7:0]								-
compsum 1 reg	0x116	FCMP1 READ[7:0]								-
lid2 reg	0x11A				LID2 READ[4:0]					-
checksum 2 reg	0x11D	FCHK2 READ[7:0]								-
compsum 2 reg	0x11E	FCMP2 READ[7:0]								-
lid3 reg	0x122				LID3 READ[4:0]					-
checksum 3 reg	0x125	FCHK3 READ[7:0]								-
compsum 3 reg	0x126	FCMP3 READ[7:0]								-
ils did	0x150	DID[7:0]								0x00
ils bid	0x151					BID[3:0]				0x00
ils lid0	0x152				LID[4:0]					0x00
ils scr l	0x153	SCR			L[4:0]					0x00
ils f	0x154	F[7:0]								0x00
ils k	0x155				K[4:0]					0x00
ils m	0x156	M[7:0]								0x00
ils cs n	0x157	CS[1:0]			N[4:0]					0x00
ils np	0x158				NP[4:0]					0x00
ils s	0x159				S[4:0]					0x00
ils hd cf	0x15A	HD			CF[4:0]					0x00
ils res1	0x15B	RES1[7:0]								0x00
ils res2	0x15C	RES2[7:0]								0x00
ils checksum	0x15D	FCHK0[7:0]								0x00
Inter lane deskew	0x160	Force Lane 1 Delay	Lane 1 interlane deskew delay[2:0]			Force Lane 0 Delay	Lane 0 interlane deskew delay[2:0]			0x00
Inter lane deskew	0x161	Force Lane 3 Delay	Lane 3 interlane deskew delay[2:0]			Force Lane 2 Delay	Lane 2 interlane deskew delay[2:0]			0x00

Register name	*Address*	*Bit7*	*Bit6*	*Bit5*	*Bit4*	*Bit3*	*Bit2*	*Bit1*	*Bit0*	*Default*
Error Counters	0x16B		Error Cnt Lane Select[2:0]					Error Cnt Cntrl Select[1:0]		0x00
Error Counters READ	0x16B	Counter value[7:0]								0x00
Lane Skew Conformance	0x16C					Enable skew conformance check[3:0]				0xFF
Registers 0x16D-0x16F have different read and write values.										
Bad Disparity Error	0x16D Write	Reset Bad Disparity Error IRQ	Disable Bad Disparity Error Counter	Reset Bad Disparity Error Counter				Bad Disparity Error Lane Address[1:0]		0x00
Bad Disparity Error READ	0x16D Read					Terminal bad disparity error[3:0]				0x00
Not in Table Error	0x16E Write	Reset Not in table IRQ	Disable Not in table Counter	Reset Not in table Counter				Not in table Lane Address[1:0]		0x00
Not in Table Error READ	0x16E Read					Terminal not in table error[3:0]				0x00
Unexpected Kchar	0x16F Write	Reset Unexpected Kchar IRQ	Disable Unexpected Kchar Counter	Reset Unexpected Kchar Counter				Unexpected Kchar Lane Address[1:0]		0x00
Unexpected Kchar READ	0x16F Read					Terminal unexpected Kchar[3:0]				0x00
Code Group Sync Flag	0x170	Reset Code Group Sync IRQ				Code Group Sync Flags[3:0]				0x00
Frame Sync Flag	0x171	Reset Frame Sync IRQ				Frame Sync Flags[3:0]				0x00
Good Checksum Flag	0x172	Reset Good Checksum IRQ				Good Check Sum Flags[3:0]				0x00
Initial Lane Sync Flag	0x173	Reset Initial Lane Sync IRQ				Initial Lane Sync Flags[3:0]				0x00
Lane skew out of range	0x174	Reset Interlane Deskew				Skew Out Of Range[3:0]				0x00

Register name	*Address*	*Bit7*	*Bit6*	*Bit5*	*Bit4*	*Bit3*	*Bit2*	*Bit1*	*Bit0*	*Default*
status		Interrupt								
Deframer Control Register 0	0x175	Disable Reciever	Disable Character Replacement		ILD reset	Deframer Soft Reset	Force Sync Request	ERPT Sync Single Error		0x00
Deframer Control Register 1	0x176	Bytes Per Frame[7:0]								0x00
Deframer Control Register 2	0x177	Link Layer testmode	Sync On Lane0	Muxin[1:0]		Multi cfg deframer octet control[1:0]		MuxOut[1:0]		0x00
Multiframes during ILAS	0x178	kval[7:0]								0x01
Invalid Define	0x179							Unexpected Kchar is invalid	Not in table is invalid	0x00
IRQ Vector/Mask	0x17A	Bad Disparity Error	Not In Table Error	Unexpected Kchar	Skew out of range	Bad ILS sequence	Bad Check Sum	Frame Sync Fail	Code Group Sync Fail	0x00
Sync Assertion Mask/Control	0x17B	Assert SYNC at Bad Disparity Error	Assert SYNC at Not In Table Error	Assert SYNC at Unexpected Kchar	Configuration Mismatch IRQ	Enable config mismatch IRQ	Number of A char multiframes[2:0]			0x08
Error Threshold	0x17C	Error threshold[7:0]								0xFF
Lane Enable	0x17D					Logical Lane enable[3:0]				0x01

REGISTER DESCRIPTIONS

WARNING: **Unspecified registers are unused/reserved and should not be written to. Reading from unused register may give unexpected results.**

Register Name	Address	Bit (Hex)	Name	Function	Default
Comm Register	00	7	SDIO	Serial data bi-directionality 0=unidirectional separate SDI and SDO (4-wire SPI), 1=Not used	0
		6	LSB/MSB-first	SPI communication LSB or MSB first 0=MSB first 1=LSB first	0
		5	Software reset	Software reset. 1=reset, must be written to 1 then written to 0	0
		4	Long Mode	Long addressing mode 0=7 bit addressing 1=15 bit addressing	0
Power Control Register	01	7	Power down DAC1	Power down DAC I 1=power down	0
		6	Power down DAC2	Power down DAC Q 1=power down	0
		5	Power down Voltage Reference	Power down the voltage reference 1=power down	0
		4	Reserved	Always set to 1	1
		3	Reserved		0
		2	Reserved		0
		1	Power down Clock Receivers	Power down the Clock Receivers 1=power down	0
		0	Txen from SPI	Control Tx enable function from SPI bit 1=enable 0=disable	1
SERDES SPI Status	02	0	SERDES deframer SPI writes allowed	During power-up and reset, writes to the deframer section of the SPI map are not allowed. This status bit can be polled to determine when SPI write to the deframer are allowed. (Alternatively the SERDES PLL Lock interrupt 0x007[6] can be used).	0
Data format Register	03	7	Binary Enable	Input data format 0= 2's complement format 1 = binary format)	0
		2	Poll/Interrupt	Disable interrupt output pin to allow polling of interrupts only 1=disable	0
		1	Single DAC	Enable only the I DAC datapath and DAC 0=disable 1=enable,	0
		0	I/Q DAC SPI select	Select either I or Q DAC SPI registers for read/write where multiple pages are used (e.g. addresses 028-02F) 0=I DAC 1=Q DAC	0
Interrupt Enable Register 0	04	7	Enable PLL	Enable interrupt for PLL lock lost	0

Register Name	Address	Bit (Hex)	Name	Function	Default
			Lock Lost	1=enable	
		6	Enable PLL Lock	Enable interrupt for PLL lock lost 1=enable	0
		4	Enable Align pin Locked	Enable interrupt for multi-chip ALIGN pin locked 1=enable	0
		3	Enable A-character out of range	Enable interrupt if /A/character alignment machine has detected the /A/character out of correctable range 1=enable	0
		2	Enable SYNCb auto cal' done	Enable interrupt for SYNCb auto calibration complete 1=enable	0
		1	Enable FIFO Warning #1	Enable interrupt for FIFO collision warning #1 (FIFO read and write pointers within 1 count) 1=enable	0
		0	Enable FIFO Warning #2	Enable interrupt for FIFO collision warning #2 (FIFO read and write pointers within 2 counts) 1=enable	0
Interrupt Enable Register 1	05	7	Enable BIST done	Enable interrupt for BIST done 1=enable	0
		6	Enable BIST done	Enable interrupt for BIST compare pass 1=enable	0
		5	Enable BIST compass fail	Enable interrupt for BIST compare fail 1=enable	0
		4	Enable AED compare pass	Enable interrupt for SED auto mode pass 1=enable	0
		3	Enable AED compare fail	Enable interrupt for SED auto mode fail 1=enable	0
		2	Enable AED compare fail	Enable interrupt for SED compare fail 1=enable	0
		1	Enable PLL band lost	Enable interrupt for PLL band lost 1=enable	0
		0	Enable PLL band lock	Enable interrupt for PLL band lost 1=enable	0
Interrupt Enable Register 2	06	7	Enable SERDES PLL Lock Lost	Enable interrupt for SERDES PLL Lock Lost 1=enable	0
		6	Enable SERDES PLL Locked	Enable interrupt for SERDES PLL Locked 1=enable	0
		1	Enable BER finished	Enable Bit Error Rate tester finished 1=enable	0
		0	Enable BER count max max	Enable Bit Error Rate tester count at maximum value (0xFFFF) 1=enable	0

Register Name	Address	Bit (Hex)	Name	Function	Default
Interrupt Status register 0[1]	07	7	Service PLL Lock Lost	Service interrupt for PLL lock lost	
		6	Service PLL Lock	Service interrupt for PLL lock	
		4	Service Align pin Locked	Service interrupt for Align pin locked	
		3	Service A-Align out of range	Service interrupt for A-character alignment machine has detected the A-character out of correctable range.	
		2	Service SYNCb auto cal done	Service interrupt for SYNCb auto calibration complete.	
		1	Service FIFO Warning #1	Service interrupt for FIFO collision warning #1 (FIFO read and write pointers within 1 count).	
		0	Service FIFO Warning #2	Service interrupt for FIFO collision warning #2 (FIFO read and write pointers within 2 counts)	
Interrupt Service Register 1	08	7	Service BIST done	Service interrupt for BIST done	
		6	Service BIST compare pass	Service interrupt for BIST compare pass	
		5	Service BIST compass fail	Service interrupt for BIST compare fail	
		4	Service AED compare pass	Service interrupt for SED auto mode pass	
		3	Service AED compare fail	Service interrupt for SED auto mode fail	
		2	Service SED compare fail	Service interrupt for SED compare fail	
		1	Service PLL band lost	Service interrupt for PLL band lost	
		0	Service PLL band lock	Service interrupt for PLL band lock	
Interrupt Status register 0	09	7	Service SERDES PLL Lock Lost	Service interrupt for SERDES PLL lock lost	
		6	Service SERDES PLL Lock	Service interrupt for SERDES PLL lock	
		1	Service FIFO Warning #1	Service interrupt for Bit Error Rate tester finished	
		0	Service FIFO Warning #2	Service interrupt for Bit Error Rate tester count at maximum value (0xFFFF)	
SYNCb control Register #1	0A	7	Enable Serial Input Link	Enable the SERDES link 1=enable	0
		6	Delay SYNCb	Enable the internal SYNCb delay. Set this bit to	1

[1] All bits are high when interrupt is active. Clear interrupt by writing respective service bit HIGH. Reading these bits when interrupt enable is not set reads back the instantaneous value of the triggering event

Register Name	Address	Bit (Hex)	Name	Function	Default
				delay SYNCb falling edge to the properly mapped phase of the internal multi-frame counter. This is needed for latency locking and multichip alignment.	
		5	SYNCb polarity	Polarity of SYNCb output pad 0 = uninverted, default value 1 = inverted)	0
		4	Autocal SYNCb delay offset	Enable auto calibration of the SYNCb delay offset 1=enable	0
		2	Enable SYNCb #1 pad output	Enable SYNCb output driver on pins 9 and 10 1=enable	1
		1	Enable SYNCb #2 pad output	Enable the auxiliary SYNCb output driver on pins 12 and 13. This bit is reserved for future use, to enable daisy-chaining or drive a second FPGA (1=enable)	0
		0	Enable SYNCb input	Enable SYNCb input receiver on pins 29 and 30. This input is used in daisy-chaining (1=enable)	0
Sync control and status Register #2	0B	7	SYNCb delay DLL enable	Enable delay DLL on the SYNCb output. Used for fine tuning of the SYNCb interface (1=enable)	0
		6	SYNCb DLL locked	SYNCb DLL is locked if set high 1=SYNCb DLL locked	0
		5	SYNCb launch from Frame falling edge	For coarse tuning of the SYNCb interface 1= launch the SYNCb from the Frame input falling edge	000
		[4:2]	SYNCb delay offset	SYNCb delay offset in two's compliment format: 100 = -4 steps, 011 = +3 steps. 000 = similar delay to launching SYNCb from frame edge.	00
		[1:0]	SYNCb timing control	Test-mode to be used in conjunction with FPGA to select best point for SYNCb launch. If set to 1, 2, or 3, the SYNCb will emit a periodic signal on the SYNC. 00 = Normal SYNCb launch mode. 01 = Frame Clock/2 periodic waveform 10 = Frame Clock/4 period Waveform 11 = Frame clock/8 Periodic waveform	
Align control register #1	0C	7	DAC align buffer enable	DAC alignment input buffer enable. 1=enable If PLL used, this buffer is at the DACCLK input, and if PLL is disable, it is at the REFCLK input.	0
		6	Use rising edge DAC Align	Use rising or falling edge of ALIGN input for DAC alignment. 0=falling 1=rising,	1
		5	Align based on Frame reference	Enable multi-chip alignment based on the Frame Source clock. If REFCLK is used for Frame, then this is the source. Frame Source clock will sample DACALIGN and then DACCLK will sample single	0

Register Name	Address	Bit (Hex)	Name	Function	Default
				pulse of Frame Source. 1=enable	
		4	Align input sampled by DACCLK rising edge	DACALIGN signal sampled by DACCLK rising edge or DACCLK falling edge. 0=falling edge 1=rising edge, If 0x0OC bit 5 is high, the Align signal is generated from the Frame Source.	1
		2	Align to Frame request	Request a multi-chip alignment to the Frame source (1). The action of writing this bit causes the request, readback of this bit is always zero.	0
Align control register #2	0D	2:0	DAC phase adjustment	DAC clock phase adjustment during alignment operation, in 2s complement format. This is limited to (interpolation rate – 1) steps internally regardless of the value written: 100 = -4 phase steps 011 = +3 phase steps	0
Align status	0E	7:0	Align status	Readback of the internal status of the alignment logic	
Datapath Control	0F	6	Bypass InvSinc	Inverse sinc filter bypass. 1=bypass	1
		5	Bypass Phase, Digital Gain and Offset Adjustment	Bypass digital phase, gain and offset adjustment. 1=bypass	1
		4	Bypass fs/4 modulation	Bypass the post-datapath fs/4 modulation 1=bypass	1
		[3:0]	Filter and NCO mode control	0000 = 1x mode, no NCO 0001 = 2x, first filter, no NCO 0010 = 2x, first filter, NCO 0011 = 2x, second filter, no NCO 0100 = 2x, second filter, NCO 0101 = 4x, no NCO 0110 = 4x, NCO 0111 = 8x, no NCO 1000 = 8x, NCO	0000
SERDES PHY configuration	10	5	RCAL_EN	Enable internal resistance calibration for CDR. 1=enable	1
		4	VTT_BUF_ENABLE	Enable the internal CDR termination voltage buffer	0
		[3:0]	VTT_BUF_CTRL	Internal control for VTT buffer. 0000 = Ground 0001 = 0.6V 0002=0.65V (steps of 0.05V 1111 = 1.3V	0000
SERDES PHY configuration	11	4:0	FRCAL	Force RCAL calibration value	0
SERDES PHY configuration	12	[7:6]	SERDES output lane matrix	01= I output on deframer rxdata[15:0] and Q on rxdata[31:16]. 10 = swap I and Q on 01 setting 00 = I on both DACs 11 = Q on both DACs	01

Register Name	Address	Bit (Hex)	Name	Function	Default
		[3:0]	HRX_ENABLE/ LANE ENABLE	CDR enable for each physical lane.Bits 0:3 correspond to lanes 0:3. 1=enable	1111
/A/ character alignment status/control	13	7	/A/ character out of range	/A/ character is out of correctable range.	
		5	Auto Calc	Finds optimal latency configuration when TX latency is not set. This bit in conjunction with read-back of 15 allows user to measure "TX latency" of FPGA. 1=enable	0
		[4:0]	Discrepancy register	/A/ alignment discrepancy register: reports how much shift register has moved from default center value	
Latency register #1	14	[4:0]	TX latency register	User has to enter the SYNCb transmit latency in FPGA/ASIC. Used for multi-chip synchronization	0
Latency register #2	15	[4:0]	Additional latency	Additional latency supplied by user to make total latency a multiple of the frame length. Readback is additional latency calculated during SYNCb autocal.	0
XBAR support	16	[7:0]	SERDES input lane matrix	SERDES input lane matrix. Control for the input cross-bar that maps logical to physical lanes. (2 bits per lane, default for four lanes is 11,10,01,00 or E4. This maps logical lane 0 to physical lane 0, and so on).	xE4
SERDES PHY configuration	17	[7:4]	SERDES symbol reverse	SERDES symbol reverse MSB to LSB: used if serialization in transmit system reverses symbols. 1=enable	0x0
		{3:0}	SERDES symbol bit invert	SERDES symbol bit invert, used if logical to physical connection to the AD9128 has reversed + and - inputs to the CDR. 1=enable	0x0
PLL Control register #1	18	7	PLL Enable	Enable PLL clock multiplier. 1=enable	0
		6	PLL Manual Enable	Enable PLL band manual selection mode. 0=Auto 1=Manual	1
		[5:0]	Manual Band	Selects the PLL band used in manual mode	0
Clk Receiver Control Register	19	7	DACCLK Duty Correction	Enable duty cycle correction on DAC clock input (1=enable)	0
		6	REFCLK Duty Correction	Enable duty cycle correction on REF clock input. 1=enable	0
		5	DACCLK Cross Correction	Enable differential crossing correction on DAC clock input. 1=enable	1
		4	REFCLK Cross Correction	Enable differential crossing correction on REF clock input. 1=enable	1
		3	Manual Cross	Enable manual setting of crossing correction.	1

Register Name	Address	Bit (Hex)	Name	Function	Default
			Sign	1=enable	
		[2:0]	Manual Cross Amplitude	Manual crossing correction value	0x7
PLL Control Register #3	1A	[7:6]	Divider 2	PLL Controller divider. 00 = 2 01 = 4 10 = 8 11 = 16	11
		4	PLL Cross Control Enable	Enable PLL Cross Point Control. 1=enable	0
		[3:2]	Divider 0	DAC clock to Data Rate divider. 00 = 2 01 = 4 10 = 8 11 = 16	01
		[1:0]	Divider 1	DAC clock to Data Rate divider. 00 = 2 01 = 4 10 = 8 11 = 16	01
PLL Status Register #1	1B	7	PLL Lock	Status indicator: PLL clock multiplier output is stable.	
		[3:0]	PLL Control Voltage Readback	PLL VCO control voltage readback value.	
SERDES PLL control register #1	1D	7	Power down frame input buffer	Power down frame input buffer. 1=power down	0
		6	Frame source reference input	Use the PLL reference clock input as the Frame clock. 1=enable	0
		5	Frame source internal	Use an internally generated Frame clock -derived from the DAC clock. 1=enable	0
		4	Frame locked to datarate counter	Use a Frame clock locked to the data rate counter or unlocked. 0 = unlocked 1=data rate counter	0
SERDES PLL control/status register #2	1E	7	SERDES DLL lock override	Override the SERDES DLL lock. 1=enable	0
		6	SERDES PLL lock	If high, indicates that SERDES PLL is locked	0
		5	SERDES PLL lock override	Override the SERDES PLL lock. 1=override	0
		4	SERDES PLL power down	Power down the SERDES PLL. 1=power down	0
		[3:0]	SERDES pclk divider ratio	SERDES PLL multiplier clock ratio	0001
Chip ID	1F	7:0	CHIP ID	Identifies the device as AD9128	0x09

Register Name	Address	Bit (Hex)	Name	Function	Default
FTW low	20	7:0	Frequency Tuning Word	NCO frequency tuning word LSBs	0
FTW mod low	21	7:0	Frequency Tuning Word	NCO frequency tuning word mid LSBs	0
FTW mid high	22	7:0	Frequency Tuning Word	NCO frequency tuning mid MSBs	0
FTW high	23	7:0	Frequency Tuning Word	NCO frequency tuning word MSBs	0
NCO phase offset low	24	7:0	Phase Offset	NCO phase offset LSBs	0
NCO phase offset high	25	7:0	Phase Offset	NCO phase offset MSBs	0
NCO FTW updating	26	0	SPI FTW Request	Update NCO FTW when set high	0
For register addresses 28-2F: DAC Address 0x003<0> = 0 for I DAC, DAC Address 0x003<0> =1 for Q DAC					
Phase Word low	28	7:0	Phaseword <7:0>	Digital Phase adjustment LSBs	0
Phase Word high	29	3:0	Phaseword <11:8>	Digital Phase adjustment MSBs	0
DC Offset low	2A	7:0	DC Offset<7:0>	Digital Offset LSBs	0
DC Offset high	2B	7:0	DC Offset <15:8>	Digital Offset MSBs	0
DC Gain	2C	7:0	Digital Gain	Digital Gain adjustment	40
Dac Gain Adj	2D	7:0	Analog FS DAC Gain Adj<7:0>	Analog Full-Scale DAC gain adjustment (LSB part)	F9
Dac Control	2F	7	Reserved		0
		6	Reserved		0
		[4:3]	Analog FS DAC Gain Adj<9:8>	Analog Full-Scale DAC gain adjustment (MSB part)	01
		[1:0]	Reserved		00
BER test control/status register	30	7	BER finished	Bit error rate (BER) test has finished (1=BER finished)	
		6	BER continuous	Start/finish BER tester in continuous mode. The action of setting this bit to 1 first starts and then finishes the BER test and counting of PRBS errors. The error count is frozen when the mode is stopped (by setting to 0).	0
		5	BER begin	Start BER tester in timed mode (The action of writing 1 to this bit first starts the BER test and counting of PRBS errors. The error count is frozen when the error period is reached as defined by the BER period select.	01
		[4:0]	BER period select	BER test timed period selections 00000 = divide by 2^37 00001 = divide by 2^38 00010 = divide by 2^39 00011 = divide by 2^40 00100 = divide by 2^41	00000

Register Name	Address	Bit (Hex)	Name	Function	Default
				00101 = divide by 2^42 00110 = divide by 2^43 00111 = divide by 2^44 01000 = divide by 2^15 (test mode) 10000 = divide by 2^14 (test mode) 11000 = divide by 2^15 (test mode)	
BER count register #1	31	[7:0]	BER count LSBs	BER error count (LSBs)	
BER count register #2	32	[7:0]	BER count MSBs	BER error count (MSBs)	
TX enable control register	33	7	PD VREF	When Txen enable is low, power down the voltage reference. 1=power down	0
		6	PD clock receivers	When Txen enable is low, power down the clock receivers. 1=power down	0
		5	PD DACs	When Txen enable is low, power down the DACs. 1=power down	0
		4	PD CDRs	When Txen enable is low, power down the SERDES CDRs. 1=power down	0
		3	PD FIFO and deframer	When Txen enable is low, power down the FIFO and deframer. 1=power down	0
		2	PD datapath	When Txen enable is low, power down the datapath. 1=power down	0
		1	Extend rising edge Txen	When Txen enable in high, extend the Txen period internally. 1=enable	0
		0	Txen rising edge extend length	Extend the Txen internally by 100us or 200us.0=100us 1=200us	0
Sample test control/status register	34	1	Sample test error/reset	Read of this bit indicates if a sample test error occurred (1=occurred). The action of writing this bit to a 1 resets the sample test mode error.	0
		0	Sample test mode	Enable the JESD204A sample test mode. 1=enable	0
Deframer wrapper control register	35	0	FIFO reset	Reset the deframer wrapper FIFOs. 1=reset	0
Deframer wrapper FIFO status	36	[7:4]	FIFOs full	Deframer wrapper FIFOs full (one bit per lane)	
		[3:0]	FIFOs empty	Deframer wrapper FIFOs empty (one bit per lane)	
CDR equaliser/CDR control register #2	3B	[3:0]	CDR EQ	Enable equalizers for each of the physical lanes. Rx0 is Bit [0] and Rx3 is bit[3]. 1=enable	0F
SERDES PRBS control register	3D	7	PRBS error output enable	Enable for PRBS output to SYNCB2 output (1=enable)	0
		[6:5]	PRBS lane select	Select PRBS lane input. 00=lane 0	00

Register Name	Address	Bit (Hex)	Name	Function	Default
				01=lane 1 10=lane 2 11=lane 3	
		4	PRBS enable	Enable PRBS tester. 1=enable	0
		3	PRBS hold pattern	Hold PRBS pattern. 1=hold	0
		[2:1]	PRBS select mode	Select PRBS polynomial. 00=2^7+2^6+1 01=2^15+2^14+1 10=2^31+2^28+1 11= PRBS hold or idle mode.	00
FIFO Therm	40	7:0	FIFO phase thermometer	Indicates how full the datapath FIFO is 00000000 = empty 11111111 = full	
Datapath FIFO control register	41	7	SPI based FIFO write side reset	SPI based FIFO write side reset (1=reset)	0
		6	SPI based FIFO write side acknowledge	SPI based FIFO write side acknowledge. 1=enable	0
		5	FIFO force data test mode	Force sinewave data in FIFO test mode. 1=enable	0
		[2:0]	FIFO WR phase offset	FIFO WR phase offset	100
Latency measurement compare value register #1	42	[7:0]	Latency compare value <7:0>	Latency compare value <7:0>	0x00
Latency measurement compare value register #2	43	[7:0]	Latency compare value <15:8>	Latency compare value <15:8>	0x00
+SERDES PLL control	50	[5:3]	Charge pump division factor		0
PRNG control	54	[7:4]	PATTTYPE	BIST/Pseudo-random number generator mode. 0001 = use device input data in BIST 0010 = noise generation mode, no capture 0100 = run forever, ignore terminal count 1000 = flush datapath to zero after test	0000
		3	PATTENA	Enable Psuedo-random number generator in BIST testing. 1=enable	0
		0	BISTENA	Built-in self test (BIST) enable (1=enable)	0
Padd_L	55	[7:0]	PattPad<7:0>	Padding length register, number of 0's before 1st pattern (LSB part)	00
Padd_H	56	[7:0]	PattPad<15:8>	Padding length register, number of 0's before 1st pattern (MSB part)	00
Patt_L	57	[7:0]	PattLen<7:0>	Pattern length register, number of patterns in BIST sequence (LSB part)	00
Patt_M	58	[7:0]	PattLen<15:8>	Pattern length register, number of patterns in BIST	00

Register Name	Address	Bit (Hex)	Name	Function	Default
				sequence (middle part)	
Patt_H	59	[7:0]	PattLen<23:16>	Pattern length register, number of patterns in BIST sequence (MSB part)	00
Sign_Ctrl	5A	7	Sign Rde	Enable read of signature register. 1=enable	0
		5	Sign Zero	Enable the don't capture on zero data logic (useful for external data mode) 1=enable)	0
		4	Sign Rnd	Randomization of signature enable. 1=enable	0
		[2:1]	Sign Sel	Selection of output source of signature. 00 = First DAC pair, I-DAC, sub-datapath A 01 = First DAC pair, I-DAC, sub-datapath B 10 = First DAC pair, Q-DAC, sub-datapath A 11 = First DAC pair, Q-DAC, sub-datapath B	00
		0	Sign Ena	Enable signature. 1=enable	0
Sign Select<1:0>= 2'bxx chooses between the subsequent four signature outputs [Reg 0x05A[2:1]					
SignOut_L	5B	[7:0]	SignOut<7:0>	Signature expected value (LSB part)	Read-only
SignOut_M	5C	[7:0]	SignOut<15:8>	Signature expected value (mid part)	Read-only
SignOut_H	5D	[7:0]	SignOut <23:16>	Signature expected value (MSB part)	Read-only
Sign Expect Status	5E	[7:4]	Exp Pass	Signature expected value pass/fail flags (one per signature).	Read-only
		[3:0]	Exp Fail		Read-only
Prng Status register	5F	6:0	Prng Status	Internal BIST state machine status (test/debug only)	
SED control/status register	63	7	SED compare enable	Enable SED data comparison (1=enable)	0
		5	SED compare fail	SED comparison failed flag	0
		3	AED compare enable	Enable AED data comparison (1=enable)	
		1	AED compare fail	SED comparison failed flag	0
		0	AED compare pass	AED comparison passed flag	
SED value register	64	7:0	SED value	Sample_Error_Detect_Pattern_1<7:0>	0x00
SED value register	65	7:0	SED value	Sample_Error_Detect_Pattern_1<15:8>	0x00
SED value register	66	7:0	SED value	Sample_Error_Detect_Pattern_2<7:0>	0x00
SED value register	67	7:0	SED value	Sample_Error_Detect_Pattern_2<15:8>	0x00
SED value register	68	7:0	SED value	Sample_Error_Detect_Pattern_3<7:0>	0x00
SED value register	69	7:0	SED value	Sample_Error_Detect_Pattern_3<15:8>	0x00

Register Name	Address	Bit (Hex)	Name	Function	Default
SED value register	6A	7:0	SED value	Sample_Error_Detect_Pattern_4<7:0>	0x00
SED value register	6B	7:0	SED value	Sample_Error_Detect_Pattern_4<15:8>	0x00
SED status register	6C	7:0	SED status	SED_Rising_Edge_Status<7:0>	
SED status register	6D	7:0	SED status	SED_Rising_Edge_Status<15:8>	
SED status register #1	6E	7:0	SED status	SED_Falling_Edge_Status<7:0>	
SED status register #2	6F	7:0	SED status	SED_Falling_Edge_Status<15:8>	
PLL Control	77	7:6	Loop filter	Select PLL loop filter bandwidth. 00 = Low 01 = Low/Medium 10 = Medium/High 11 = High	11
		[4:3]	Charge pump multiplier	PLL charge pump current multiplier. 00 = 0.5x 01 = 1x 10 = 2x 11 = 4x	01
		[2:0]	Charge pump nominal current	Set nominal PLL charge pump current. 000 =112.5µA 001 =125.0µA010 =137.5µA 011 =150.0µA 100 =162.5µA 101 =175.0µA 110 =187.5µA 111 =200.0µA	001
All registers beyond this point can only be accessed in long addressing mode. Addresses 0x100-0x126 are read-only.					
SERDES deframer configuration	100	[7:0]	DID	Device (link) identification number	Read-only
SERDES deframer configuration	101	[3:0]	BID	Bank identification number (extension of DID)	Read-only
SERDES deframer configuration	102	[4:0]	LID0	Lane Identification for lane 0	Read-only
SERDES deframer configuration	103	7	SCR	Scrambling enabled	Read-only
		[4:0]	L	Number of lanes per convertor	Read-only
SERDES deframer configuration	104	[7:0]	F	Octets per frame	Read-only
SERDES deframer configuration	105	[4:0]	K	Framer per multiframe	Read-only
SERDES deframer configuration	106	[7:0]	M	Number of converters	Read-only
SERDES deframer configuration	107	[7:6]	CS	Number of control bits per sample	Read-only
		[4:0]	N	Converter resolution	Read-only
SERDES deframer configuration	108	[4:0]	NP	Total number of bits per converter word (N+CS+tail bits).	Read-only

Register Name	Address	Bit (Hex)	Name	Function	Default
SERDES deframer configuration	109	[4:0]	S	Number of samples per converter per frame cycle	Read-only
SERDES deframer configuration	10A	7	HD	High density mode - allows converter word split across lanes.	Read-only
		[4:0]	CF	Number of control words per frame	Read-only
SERDES deframer configuration	10B	[7:0]	RES1	JESD204A reserved	Read-only
SERDES deframer configuration	10C	[7:0]	RES2	JESD204A reserved	Read-only
SERDES deframer configuration	10D	[7:0]	FCHK0	Received checksum register for lane 0 (sum of previous 13 registers modulo 0xFF)	Read-only
SERDES deframer configuration	10E	[7:0]	FCMP0	Computed checksum register for lane 0 (sum of previous 13 registers modulo 0xFF)	Read-only
SERDES deframer configuration	112	[4:0]	LID1	Lane Identification for lane 1	Read-only
SERDES deframer configuration	115	[7:0]	FCHK1	Received checksum register for lane 1 (sum of previous 13 registers modulo 0xFF)	Read-only
SERDES deframer configuration	116	[7:0]	FCMP1	Computed checksum register for lane 1 (sum of previous 13 registers modulo 0xFF)	Read-only
SERDES deframer configuration	11A	[4:0]	LID2	Lane Identification for lane 2	Read-only
SERDES deframer configuration	11D	[7:0]	FCHK2	Received checksum register for lane 2 (sum of previous 13 registers modulo 0xFF)	Read-only
SERDES deframer configuration	11E	[7:0]	FCMP2	Computed checksum register for lane 2 (sum of previous 13 registers modulo 0xFF)	Read-only
SERDES deframer configuration	122	[4:0]	LID3	Lane Identification for lane 3	Read-only
SERDES deframer configuration	125	[7:0]	FCHK3	Received checksum register for lane 3 (sum of previous 13 registers modulo 0xFF)	Read-only
SERDES deframer configuration	126	[7:0]	FCMP3	Computed checksum register for lane 3 (sum of previous 13 registers modulo 0xFF)	Read-only
SERDES deframer configuration	150	[7:0]	DID	Device (link) identification number	0
SERDES deframer configuration	151	[3:0]	BID	Bank identification number (extension of DID)	0
SERDES deframer configuration	152	[4:0]	LID	Lane Identification	0
SERDES deframer configuration	153	7	SCR	Scrambling enabled	0
		[4:0]	L	Number of lanes per converter	0
SERDES deframer configuration	155	[4:0]	K	Framer per multiframe	0
SERDES deframer configuration	156	[7:0]	M	Number of converters	0
SERDES deframer configuration	157	[7:6]	CS	Number of control bits per sample	0
		[4:0]	N	Converter resolution	0
SERDES deframer	158	[4:0]	NP	Total number of bits per converter word	0

Register Name	Address	Bit (Hex)	Name	Function	Default
configuration				(N+CS+tail bits).	
SERDES deframer configuration	159	[4:0]	S	Number of samples per converter per frame cycle	0
SERDES deframer configuration	15A	7	HD	High density mode - allows converter word split across lanes.	0
		[4:0]	CF	Number of control words per frame	0
SERDES deframer configuration	15B	[7:0]	RES1	JESD204A reserved	0
SERDES deframer configuration	15C	[7:0]	RES2	JESD204A reserved	0
SERDES deframer configuration	15D	[7:0]	FCHK0	Checksum register for lane 0 (sum of previous 13 registers modulo 0xFF)	0
SERDES deframer configuration	160	7	Force lane 1 delay	Lanes 0 and 1 inter-lane delay/skew control: Force lane 1 delay. 1=enable	0
		[6:4]	Lane 1 delay	Lane 1 delay (Write is forced value, Read is computed value)	000
		3	Force lane 0 delay	Force lane 0 delay. 1=enable	0
		[2:0]	Lane 0 delay	Lane 0 delay (Write is forced value, Read is computed value)	000
SERDES deframer configuration	161	7	Force lane 3 delay	Lanes 2 and 3 inter-lane delay/skew control: Force lane 3 delay 1=enable	0
		[6:4]	Lane 3 delay	Lane 3 delay (Write is forced value, Read is computed value)	000
		3	Force lane 2 delay	Force lane 2 delay. 1=enable	0
		[2:0]	Lane 2 delay	Lane 2 delay (Write is forced value, Read is computed value)	000
SKW_LE	16C	3:0	Skew checking lane enable	Enables for skew conformance checking. (1 bit per lane). If the skew in a particular lane(s) do not fall within the permissible skew budget across all lanes, the corresponding bit is set and reported via this register.	1111
Bad disparity	16D	7	Reset IRQ	Reset Bad Disparity IRQ. 1=reset	0
		6	Disable error count	Disable Bad Disparity error count 1=disable	0
		5	Reset count	Reset Bad Disparity error count. 1=reset	0
		{2:0}	Lane address	Bad Disparity error lane address	000
Note The write values for this register are described above. The read value for this register is the Bad Disparity error count for the given lane address.					
Not-in-table character	16E	7	Reset IRQ	Reset NIT IRQ.	0

Register Name	Address	Bit (Hex)	Name	Function	Default
(NIT)				1=reset	
		6	Disable error count	Disable NIT error count. 1=disable	0
		5	Reset count	Reset NIT error count. 1=reset	0
		{2:0}	Lane address	NIT error lane address.	000
Note: The write values for this register are described above. The read value for this register is the NIT error count for the given lane address					
Not-in-table character (NIT)	16F	7	Reset IRQ	Reset Unexpected K- character IRQ. 1=reset	0
		6	Disable error count	Disable Unexpected K- character error count. 1=disable	0
		5	Reset count	Reset Unexpected K- character error count. 1=reset	0
		{2:0}	Lane address	Unexpected K- character error lane address.	000
Note: The write values for this register are described above. The read value for this register is the Unexpected K- character error count for the given lane address.					
Code Group sync flags	170	[3:0]	Code group sync flags	Code group sync flags. (One bit per lane, write to bit 7 to reset corresponding IRQ).	0
Frame sync flags	171	[3:0]	Frame sync flags	Frame sync flags. (One bit per lane, write to bit 7 to reset corresponding IRQ).	0
Good checksum flags	172	[3:0]	Good checksum flags	Good checksum flags. (One bit per lane, write to bit 7 to reset corresponding IRQ).	0
Initial lane sync flags	173	[3:0]	Initial lane sync flags	Initial lane sync flags. (One bit per lane, write to bit 7 to reset corresponding IRQ).	0
Skew outside range status register	174	[3:0]	Skew outside range	Skew during ILAS is outside permissible skew budget (one bit per lane).	-
Deframer control register #0	175	7	Disable the deframer	Disable the deframer. 1=disable	0
		6	Disable character replacement	Disable /A/ and /F/ character replacement. 1=disable	0
		4	Reset ILD logic	Reset the inter-lane de-skew logic. 1=reset	0
		3	Deframer soft reset	Soft reset the deframer internal state, doesn't affect the deframer SPI registers. 1=reset	0
		2	Force SYNCb	Force SYNCb signal from deframer low. 1=enable	0
		1	SYNCb error reporting	Use SYNCb for error reporting mode. 1=enable	0

Register Name	Address	Bit (Hex)	Name	Function	Default
			mode		
		0	Reserved		
Deframer control register #1	176	[7:0]	Bytes per frame	Software value of F if different value used to generate the deframer logic (32)	
Deframer control register #2	177	7	ILS mode	JESD204A data link layer test mode (5.3.3.9.2). 1=enable	0
		6	SYNCb on lane0 only	SYNCb generated on lane 0 only or on all lanes. 0 = all lanes 1 = lane 0	0
		[5:4]	Input lane mapping	Mapping of receiver data from lower lanes mapped to other lanes. 1=enable)	0
		[3:2]	Deframer octet counter config'	Multi-configuration deframer octet counters control.	0
		[1:0]	Output lane mapping	Mapping of deframer output samples to deframer outputs.	0
Kval register	178	[7:0]	KSYNC	Number of 4*K multiframes during ILS (must be set to 2 when 0x17B bit 0 is set to 1)	1
Invalid define register	179	1	UEKC_ENA	Enables INVALID symbol to include unexpected K-char in user data. 1=enable	0
		0	NIT_ENA	Enables INVALID symbol to include NIT symbols in user data. 1=enable	0
Deframer IRQ status/mask register	17A	7	BAD disparity	BAD disparity interrupt enable/readback	1
		6	Not-in-table error	Not-in-table interrupt enable/readback	1
		5	Unexpected K-char	Unexpected K-char interrupts enable/readback	1
		4	Inter-lane deskew	Inter-lane deskew interrupt enable (informative)	1
		3	Initial lane sync state machine flag	Initial lane synchronization state machine interrupt enable (informative)	1
		2	Good check sum flag	Good check sum interrupt enable (informative)	1
		1	Frame SYNC state machine flag	Frame SYNC state machine interrupt enable (informative)	1
		0	Code Group Sync flag	Code Group synchronization interrupt enable (informative)	1
Note: Write 1 to set interrupt mask, read to get interrupt status.					
SYNCb rising mask and control register	17B	7	Bad disparity	Enable SYNC request on Bad Disparity count reaching threshold 1=enable	1
		6	Not-in-table error	Enable SYNC request on Not-in-table error count reaching threshold.	1

Register Name	Address	Bit (Hex)	Name	Function	Default
				1=enable	
		5	Unexpected K-char	Enable SYNC request on Unexpected K-char count reaching threshold. 1=enable	1
		4	Configuration mismatch	Reset configuration mismatch interrupt when written, configuration mismatch status when read. 1=reset	0
		3	Configuration mismatch interrupt	Enable configuration mismatch interrupt. 1=enable	1
		[2:1]	Reserved		
		0	Multi-chip alignment/Latency lock	Enables multi-chi alignment/latency locking in deframer. When enabled, register 0x178 must be set to 2. 1=enable	000
Error threshold	17C	7:0	Error Threshold	Bad disparity, Not-in-table and Unexpected K-character errors are counted and compared to this error threshold and can either create an interrupt or SYNCb rising depending on registers above.	0xFF
Lane enable	17D	3:0	Lane Enable	Mask of lanes into the deframer	0x01

OUTLINE DIMENSIONS

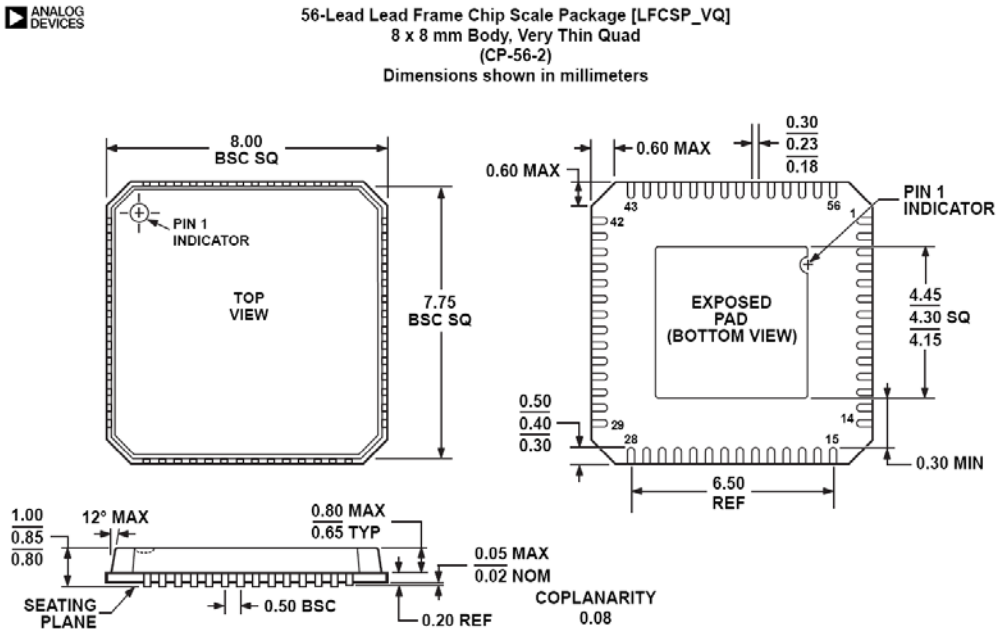


Figure 48.
56-Lead Thin Quad Flat Package, Exposed Pad [LFCSP_VQ]
(CP-56-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option

PR10871-0-6/12(Prl)